Amplitude-Regulated Quadrature Sine-VCO Employing an OTA-C Topology

Swagat Bhattacharyya, *Graduate Student Member, IEEE,* and David W. Graham, *Senior Member, IEEE*

***Abstract*—Transconductance amplifier capacitor oscillators (TACOs) readily produce phase-shifted sinusoids with low distortion over a wide frequency range. Hence, TACOs can be used in applications including telecommunications and lock-in amplifiers. The precise amplitude regulation needed in such applications necessitates an automatic gain controller (AGC) with an envelope detector. TACOs and envelope detectors have frequency-dependent nonidealities which complicate AGC design and incite amplitude modulation outside a limited frequency range. This work presents a VCO with an AGC that uses maxima sampling to compensate for envelope detector nonidealities. The VCO, which is evaluated using a field-programmable analog array, is tunable from $30\,\mathrm{Hz}$ to $40\,\mathrm{kHz}$ and consumes $\leq 50\,\mu\mathrm{W}$.**

***Index Terms*—Sine-VCO, AGC, low-power, envelope detector, OTA-C, TACO, pole-placement, maxima sampling**

I. Introduction

PHASE-SENSITIVE circuits for signal processing often require a quadrature sinusoidal oscillator with a readily tunable output amplitude and a wide output frequency range. Direct digital synthesis (DDS) can conveniently generate such sinusoids; however, DDS quantizes output amplitude, frequency, and phase, producing undesired aliasing in demodulation applications. DDS also requires a large number of components for good resolution and high bandwidth [1], and memory overhead grows exponentially with resolution [2].

In contrast, low-power operational transconductance amplifier capacitor (OTA-C) circuits known as transconductance amplifier capacitor oscillators (TACOs) readily produce sinusoids without quantization artifacts [3]. TACOs have been successful in applications such as soil impedance analyzers [4]. TACOs can produce the quadrature reference signals needed for analog lock-in amplifiers, which can be used in precision sensing applications like bioimpedance measurement [5] or vibration monitoring [6]. The last three decades have brought forth work enumerating TACO configurations [3, 7], demonstrating wide frequency tuning (up to seven decades) [8], and exhibiting designs with special output phases [4, 9].

Despite the potential utility of TACOs, ensuring constant output amplitude over the wide frequency range of TACOs has proven challenging. Reference signals for phase-sensitive signal processors, such as lock-in amplifiers, need precise amplitude control because the output scales with the reference amplitude and large oscillation amplitudes can force the comprising OTAs beyond their linear range, causing distortion.

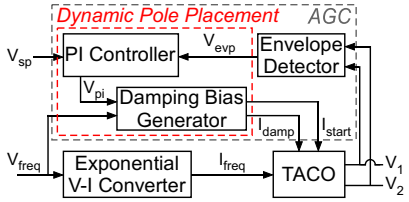

Fig. 1. Block diagram of the proposed VCO. The TACO produces the oscillations, while the auxiliary components control the frequency and amplitude.

Two amplitude-control approaches have been introduced: native amplitude limiting [10, 11] and automatic gain control (AGC) [3, 4], both of which have achieved total harmonic distortion (THD) below 0.5%. Native approaches leverage nonlinearities to constrain output amplitude. AGC schemes estimate output amplitude with an envelope detector and employ negative feedback to sustain the amplitude at a set point. Native approaches offer good amplitude stability with low component count but yield frequency-dependent output amplitudes. AGCs yield better amplitude tuning with lower frequency dependence but have more components and higher risk of amplitude modulation. Due to the frequency dependence of native approaches, AGC is necessary for producing constant-amplitude sinusoids over a wide frequency range.

Envelope detectors, which measure oscillation amplitude, are pivotal in AGCs [3], greatly affecting performance. Each envelope detector design has an innate tradeoff between output ripple and tracking latency, which vary with input frequency [12]. Tracking latency and ripple are unavoidable in causal, continuous-time envelope detectors, and both can incite AGC instability; envelope detectors with low ripple and tracking latency across a wide frequency range are imperative in a TACO-based voltage-controlled oscillator (VCO).

To this end, this work proposes an envelope detector using a continuous-time circuit (with low ripple at high frequencies) and a maxima-sampling circuit (with low ripple at low frequencies) in conjunction to mitigate ripple across a wide range of carrier frequencies while keeping tracking latency low. Dynamic pole placement circuits in the AGC maintain the DC voltage of the envelope detector output at a user-specified set point (V_{sp}) via the damping OTAs in the TACO, thereby regulating the output amplitude. An exponential V-I converter tunes the oscillation frequency of the TACO using input voltage V_{freq}. As shown in Fig. 1, the interactions between the exponential V-I converter, TACO, and AGC yield the quadrature sine-VCO. The VCO is implemented on the

This work was supported by the National Science Foundation under Award CNS-1148815 and by the National Science Foundation Graduate Research Fellowship under Grant No. DGE-2039655. *(Corresponding author: David W. Graham.)*

S. Bhattacharyya is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: sbhattac8@gatech.edu). D. W. Graham is with the Lane Department of Computer Science and Electrical Engineering, West Virginia University, Morgantown, WV 26506 USA (e-mail: david.graham@mail.wvu.edu)

Reconfigurable Analog Mixed-Signal Platform (RAMP), an in-house field-programmable analog array (FPAA) fabricated in a $0.35\,\mu\mathrm{m}$ CMOS process [13, 14], and VCO performance is evaluated over the audio band (approximately $20\,\mathrm{Hz}$-$20\,\mathrm{kHz}$).

The novelty of this work lies in its amplitude control approach, which involves frequency-dependent compensation for stabilizing performance across multiple frequency decades. We mitigate the ripple and latency of a continuous envelope detector at low frequencies with maxima sampling, and we scale PI controller gain with frequency. Compensation is facilitated by a highly reconfigurable FPAA. Floating-gate (FG) transistors are used to provide precise bias currents for setting time constants and to accurately trim process variations. The flexibility enabled by FGs—which can be programmed to 13 bits of precision [15, 16], remain accurate for ≥ 10 years [17], can be compensated to minimize the effects of temperature variation [18, 19], and have scaled well to a $40\,\mathrm{nm}$ process [20]—is encouraging others to revisit TACOs [17].

II. TACO and Exponential Frequency Tuning

The TACO used in this work [Fig. 2(a)] is a four-OTA, two-capacitor topology which has appeared often in the literature [3, 4, 7, 8, 10]. The OTAs composing this TACO [Fig. 2(b)] are bump-linearized [21] for a linear differential input range of $\pm 80\,\mathrm{mV}$ about midrail (Mid $= 1.25\,\mathrm{V}$ is produced externally and is factored into the power measurements), where the transconductance is proportional to the bias current: $G = K_0 I_{bp}$. Referencing TACO outputs V_1 and V_2 to midrail, which is an AC ground, yields the following small-signal expression:

$$\frac{\partial}{\partial t}\begin{bmatrix}V_1\\V_2\end{bmatrix} = \frac{1}{C}\begin{bmatrix}G_{eq} & G_m\\ \text{-}G_m & 0\end{bmatrix}\begin{bmatrix}V_1\\V_2\end{bmatrix};\ G_{eq} = G_{start} - G_{damp} \quad (1)$$

The state matrix eigenvalues (λ) are the poles of the TACO:

$$\lambda = \left(G_{eq} \pm j\sqrt{4G_m^2 - G_{eq}^2}\right)/2C \quad (2)$$

The TACO oscillates when $G_m > |G_{eq}|/2$, and its output is "quadrature" in that V_1 lags V_2 by roughly $\pi/2$ [see Fig. 3(e) for exemplary signals]. Constant amplitude, quadrature output, and a narrow spectrum about oscillation rate $\omega_0 = G_m/C$ are achieved when the real part of λ approaches zero. It is impractical to set $\mathfrak{Re}(\lambda) = 0$ due to nonlinearities and noise [3]; hence, this work introduces dynamic pole placement, whereby $\mathfrak{Re}(\lambda)$ is adjusted as needed using an AGC.

V_{freq}, the externally supplied frequency control voltage [Fig. 1], likely contains additive noise. The AGC in this work is more sensitive to additive noise than to multiplicative noise in the TACO frequency ($F_{osc} = \omega_0/2\pi$), especially at low F_{osc}. Since $F_{osc} \propto I_{freq}$, we use an exponential V-I converter to generate I_{freq}, which converts additive noise in V_{freq} to multiplicative noise in F_{osc}. The exponential V-I converter in this work is based on a circuit shown in [22] and generates I_{freq} by regulating the voltage across a diode-connected BJT.

III. Maxima-Sampling Envelope Detector

AGCs, which use envelope detectors for state estimation, can be destabilized by envelope detector ripple and tracking latency. This work requires an envelope detector with low ripple and low tracking latency over the audio band. Yet, a tradeoff exists between output ripple and latency in continuous-time envelope detectors [12]. An envelope detector biased for low tracking latency typically has high output ripple at low carrier frequencies; conversely, low output ripple at low carrier frequencies generally implies high latency. Our "maxima-sampling envelope detector" achieves both low ripple and low latency by compensating the low-frequency performance of the "magnitude detector" from [12] with a circuit that samples and holds input maxima (hereafter the "maxima S&H").

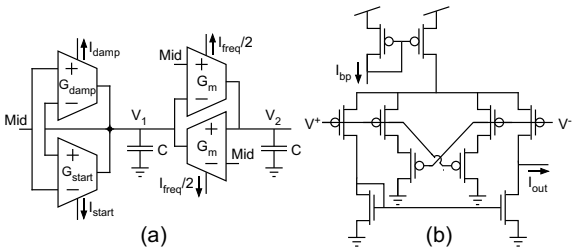

Fig. 2. (a) 4OTA2C TACO. (b) "Bump-linearized" OTA on the RAMP.

A. Envelope Detector Subcircuits

Fig. 3(a) shows our entire maxima-sampling envelope detector which comprises four subcircuits:

1) Peak Detector [12]: This is an asymmetric integrator that is biased for upper envelope tracking ($G_{P,A} \gg G_{P,D}$).

2) Adaptive-τ Filter [12]: This is a nonlinear lowpass filter with a decreasing time constant (τ) with respect to increasing input amplitude. It filters envelope detector ripple with a lower penalty to temporal accuracy compared to a linear filter.

3) S&H: This S&H has an output (V_{sh}) that tracks its input (V_{pk}) when its clock line (V_{clk}) is high and holds the previously sampled value of V_{pk} when V_{clk} is low.

4) Clock Generator: This circuit [Fig. 3(b)] generates clock pulses at V_1 maxima. The carrier of V_1 lags the carrier of V_2 by $\pi/2$ for small $\mathfrak{Re}(\lambda)$, so the clock generator logic detects when V_2 drops below midrail to identify V_1 maxima. Clock generator logic also verifies V_1 is above midrail before identifying V_1 maxima to reduce false positives if the TACO output envelope is rapidly changing. The "timer," an inverter with a tunable high-low output transition time, sets the clock pulse width: $T_{CLK} = \text{Mid} \cdot C_{TIM}/I_{TIM}$. Comparator slew causes a delay T_D from a V_1 maximum to its corresponding clock pulse. Fig. 3(c) shows V_1, V_2, and V_{clk}. A conceptually similar maxima S&H with different clock generation logic was shown in [23].

B. Operational Principles

The maxima-sampling envelope detector is formed by partitioning the "magnitude detector" (i.e. peak detector and adaptive-τ filter) from [12] with a maxima S&H [Fig. 3(a)]. For a sinusoidal input of a given frequency, the maxima S&H output voltage (V_{sh}) has a ripple that is due to the output tracking the input (V_{pk}) while V_{clk} is high. This ripple increases at high frequencies since the fixed clock pulse width (T_{CLK}) approaches the input period. The magnitude detector must be biased for a small effective time constant to minimize latency; thus, the magnitude detector has high output ripple at

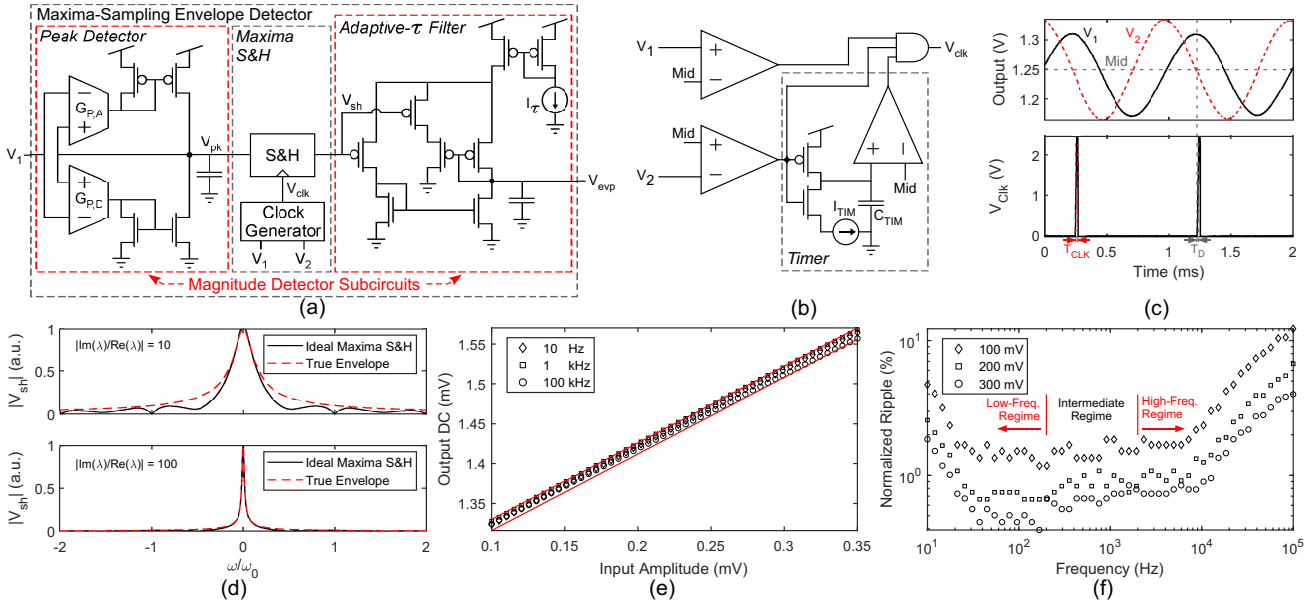

Fig. 3. (a) Maxima-sampling envelope detector schematic. (b) Clock generator schematic. (c) Plot of V_1, V_2, and V_{clk} at $F_{osc} = 1$ kHz. (d) Frequency-domain model of how $|\Im\mathfrak{m}(\lambda)/\Re\mathfrak{e}(\lambda)|$ restricts baseband estimation accuracy. (e) Measured envelope detector linearity characterization and (f) ripple characterization; the low-frequency ($\leq$200 Hz) and high-frequency ($\geq$2 kHz) regimes delimit where maxima S&H and magnitude detector behavior prevail, respectively.

low frequencies since the magnitude detector time constant approaches the input period. Due to the complementary behavior of the maxima S&H and the magnitude detector, the maxima-sampling envelope detector is biased such that overall behavior is dominated by the maxima S&H at low frequencies and by the magnitude detector at high frequencies. Overall behavior can be elucidated by separately studying the envelope detector operation at low and high carrier frequencies.

1) Low-Frequency Operation: The maxima S&H dominates overall behavior at low carrier frequencies, where the peak detector and adaptive-τ filter approximate voltage buffers since the magnitude detector time constant is smaller than the carrier period. The envelope detector input (TACO output) is narrowband; hence, the maxima S&H samples the input with a zero-order hold near carrier signal maxima (at roughly half the Nyquist rate) to estimate the baseband signal. This means that the maxima S&H sampling rate (ω_s) matches the TACO oscillation rate (i.e., $\omega_s = \omega_0 = |\Im\mathfrak{m}(\lambda)|$), producing undesired aliases which should be mitigated for proper AGC operation.

Aliasing can be studied by idealizing the maxima S&H as an impulse-train sampler that is driven at a sampling rate of ω_0 followed by a zero-order hold. Aliasing occurs when $|\Im\mathfrak{m}(\lambda)/\Re\mathfrak{e}(\lambda)|^{-1} > 0$, which corresponds to: (i) the signal envelope growing or shrinking between carrier signal periods and (ii) the input having spectral components at all frequencies. In the process of demodulation, maxima S&H sampling generates harmonics of the input signal which can seep into the baseband and corrupt the envelope estimate; the aliasing caused by these harmonics becomes more severe at lower values of $|\Im\mathfrak{m}(\lambda)/\Re\mathfrak{e}(\lambda)|$, as depicted in the frequency domain representation in Fig. 3(d). Hence, the dynamic pole placement circuits (described in Section IV) must keep TACO poles close to the imaginary axis for reliable operation.

2) High-Frequency Operation: As ω_0 increases, the duty cycle of V_{clk} increases (since pulse width T_{CLK} is fixed), thereby increasing the fraction of time the S&H is tracking its input. When the duty cycle of V_{clk} approaches 100% ($\omega_0 > 2\pi I_{TIM}/(\text{Mid} \cdot C_{TIM})$), the maxima S&H resembles a passthrough, and the magnitude detector dominates overall behavior. "Sandwiching" the maxima S&H between the peak-detector and adaptive-τ filter mitigates nonidealities since: (i) the peak detector makes maxima acquisition accuracy less sensitive to timing, and (ii) the adaptive-τ filter suppresses maxima S&H ripple, clock feedthrough, and aliases.

C. Envelope Detector Biasing

Envelope detector performance depends on proper subcircuit biasing; we bias the envelope detector for a maximally flat relation between output ripple and input carrier frequency below some target ripple (R_{TAR}). The worst-case ripple (R_{worst}) is the product of maxima S&H ripple (R_{sh}) and magnitude detector ripple (R_{mag}). The S&H input tracking period (T_{CLK}), which is regulated by clock generator bias I_{TIM} [Fig. 3(b)], is the primary cause of output ripple in a maxima S&H (disregarding leakage). I_{TIM} is chosen so T_{CLK} exceeds the S&H settling time (~20 µs in this work). If test signal $V_{pk}(t) = \cos(2\pi ft)$ is passed into the maxima S&H, analysis of the output when the S&H is tracking reveals:

$$\begin{aligned} R_{sh} &\approx \left[\cos(2\pi f T_D) - \cos(2\pi f(T_D + T_{CLK}))\right]/2 \\ &\approx (\pi f T_{CLK})^2 \text{ for } T_D \ll T_{CLK},\ f < 1/5T_{CLK} \end{aligned} \quad (3)$$

(3) shows that maxima S&H ripple grows by 40 dB/dec when $f \ll 1/5T_{CLK}$. In contrast, the ripple of the magnitude detector, a pseudo-second-order system [12], decays by 40 dB/dec above the magnitude detector ripple corner frequency (f_c).We set $f_c < 1/5T_{CLK}$ to leverage the complementary behavior of the magnitude detector and the maxima S&H, which means smaller T_{CLK} values decrease tracking latency. If the interval $(f_c, 1/5T_{CLK})$ is made sufficiently wide, there is a frequency f_{eq} ($f_c < f_{eq} < 1/5T_{CLK}$) where $R_{sh} = R_{mag} = \sqrt{R_{TAR}}$:

$$f_{eq} \approx \sin^{-1}\left(\sqrt[4]{R_{TAR}}\right)/\pi T_{CLK} \text{ for } T_D \ll T_{CLK} \quad (4)$$

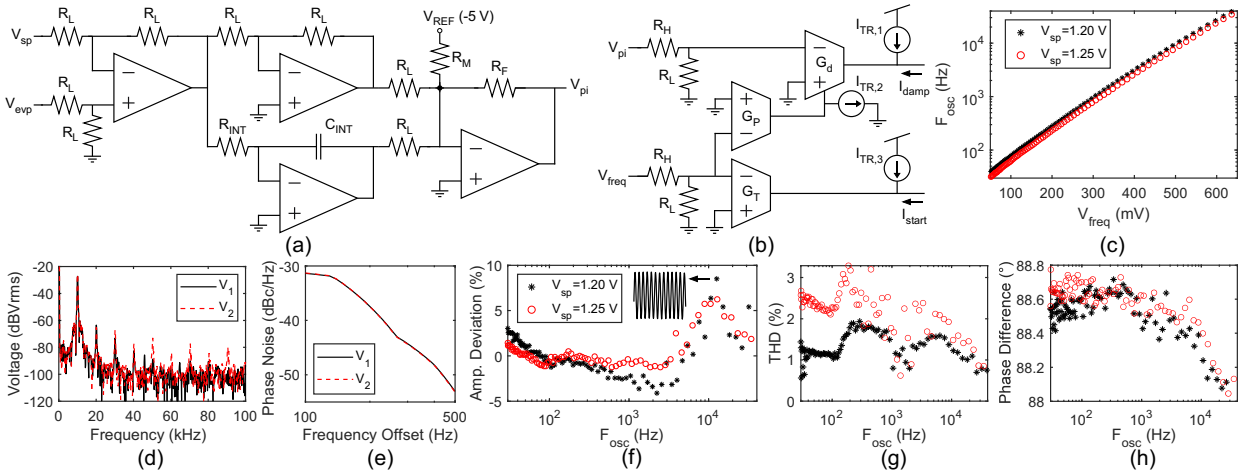

Fig. 4. (a) Off-chip PI controller; given the typical operational amplifier biases in audio-frequency applications, on-chip implementation on the RAMP would increase overall power draw by $\sim$2 µW. This work uses $R_L = 100\,\text{k}\Omega$ and $R_H = 1\,\text{M}\Omega$. (b) Damping bias generator schematic. (c) Exponential tuning of F_{osc} via V_{freq}. (d) Measured output spectrum and (e) phase noise at $F_{osc} = 10\,\text{kHz}$ and $V_{sp} = 1.20\,\text{V}$. (f) Measured amplitude deviation from mean, (g) THD, and (h) output phase difference versus F_{osc} for two values of V_{sp}. V_{sp} =1.20 V and V_{sp} =1.25 V corresponded to mean peak-peak amplitudes of 143 mV and 272 mV, respectively. Peak-peak oscillation amplitude, which is bounded by the ripple of the maxima-sampling envelope detector on the lower end and by OTA nonlinearity on the upper end, can be adjusted from 125 mV to 300 mV.

TABLE I
PERFORMANCE COMPARISON TO HISTORICAL WORK WITH AMPLITUDE REGULATION (NAL: NATIVE AMPLITUDE-LIMITING)

	Proposed (AGC)	[3] (AGC)	[4] (AGC)	[10] (NAL)	[11] (NAL)	[24] (NAL)
Technology (µm)	0.35	2	0.8	0.5	0.8	0.8
Power Draw (µW)	46-50	–	–	0.19-6.27	1050-1580	$\sim$355
THD (%)	$\leq$1.9 (V_{SP}=1.20 V)	0.2-2.8	–	$\sim$3@100 kHz	0.7-2.3	0.9@1 MHz
Frequency (MHz)	0.03-40 kHz (**3.1 dec**)	2-14 (0.8 dec)	48-132 (0.4 dec)	0.002-0.1 (1.6 dec)	1-25 (1.4 dec)	0.5-1.1 (0.3 dec)

where f_{eq} and $\sqrt{R_{TAR}}$ are input into the biasing algorithm in [12] to obtain magnitude detector biases ($R_{TAR} = 0.01$ in this work). This biasing strategy establishes three important results: (i) $R_{worst} = R_{TAR}$ in the frequency interval $(f_c, 1/5T_{CLK})$, where R_{TAR} implicitly sets the interval width, (ii) R_{worst} has a roll-off of 40 dB/dec outside $(f_c, 1/5T_{CLK})$ given an ideal S&H, and (iii) the magnitude detector is biased for a high ripple corner frequency, reducing overall tracking latency.

D. Envelope Detector Characterization

After biasing, the envelope detector shows good linearity with input amplitude [Fig. 3(e)] with a scale factor nonlinearity of 2.5% relative to a 240 mV full scale output range (measured over a four decade input frequency range). Fig. 3(f) shows envelope detector ripple versus input frequency. The envelope detector exhibits low output ripple over the audio range and an exceptionally flat ripple level from 30 Hz to 10 kHz as theorized. Additive ripple from S&H leakage and clock feedthrough, which are prominent for frequencies below 30 Hz and above 10 kHz, respectively, cause output ripple to grow (rather than decay as predicted) asymptotically. Clock feedthrough is largely due to slow clock skew in this work.

IV. Dynamic Pole Placement

Dynamic pole placement, the final element for the VCO, refers to the adjustment of equivalent transconductance $G_{eq} = G_{start} - G_{damp}$ to temporarily move TACO poles (λ) to the left or right half-plane so that the envelope estimate V_{evp} tracks user-defined set point V_{sp}. This requires $\text{sgn}\,(G_{eq})$ to track $\text{sgn}\,(V_{sp} - V_{evp})$, which is done using two circuits: the "PI controller" and the "damping bias generator."

The PI controller [Fig. 4(a)] controls G_{damp} by producing damping bias generator input V_{pi} from $e(s) = V_{sp} - V_{evp}$:

$$V_{pi}(s) = K_C\,(1 + 1/\tau_I s)\,e(s) - (R_F \cdot V_{REF})\,/R_M \qquad (5)$$

In (5), the DC gain is $K_C = -R_F/R_L$, and the integrator time constant is $\tau_I = R_{INT}C_{INT}$. We tuned τ_I using the Ziegler-Nichols method and found it to be around 1 s for our implementation. This large τ_I necessitated a large C_{INT}, resulting in the PI controller being implemented off chip using external components. R_F, R_L, and R_M are chosen so that V_{pi} spans the RAMP input range. The concept of TACO amplitude regulation via PI control was first presented in [3], and in this work, we have extended these concepts to an AGC designed to enable a multi-decade TACO frequency range.

Parasitics and nonlinearities heavily impact TACO AGC design and can be difficult to compensate [3]. Our demonstration setup is prone to parasitics from the RAMP's routing fabric; nevertheless, the RAMP's reconfigurability lets us design the "damping bias generator" [Fig. 4(b)], an empirically compensated V-I converter for generating I_{damp} and I_{start}. At a given F_{osc}, there is a minimum I_{start} value (denoted $I_{start,min}$) necessary for a self-starting TACO when $I_{damp} = 0\,\text{A}$. There is also a maximum G_d value for which the AGC is stable (denoted $G_{d,max}$). The frequency dependence of $I_{start,min}$ on the RAMP resembles a logarithm; thus, I_{start} is scaled linearly to V_{freq} so $I_{start} \propto \log\,(F_{osc}/F_{NS})$ for $F_{osc} \geq F_{NS}$. F_{NS}, set by $I_{TR,3}$, denotes the critical frequency above which the TACO is not self starting if $I_{start} = I_{damp} = 0\,\text{A}$. For similar reasons, G_d is increased linearly to V_{freq} to approximate $G_{d,max}/5$. Bias $I_{TR,1}$ compensates the input offset of G_d,

so that $I_{damp} = R_L G_d V_{pi} / (R_L + R_H)$ where:

$$G_d = K_0 \left[I_{TR,2} + R_L G_P V_{freq} / (R_L + R_H) \right] \quad (6)$$

V. Results

VCO circuits are constructed on the RAMP, a reconfigurable system fabricated in a $0.35\,\mu\mathrm{m}$ CMOS process with Vdd $= 2.5\,\mathrm{V}$ [13, 14], and the PI controller was external to the RAMP. Static biases internal to the RAMP are generated with floating-gate transistors. Control voltages V_{freq} and V_{sp} are supplied from a function generator in this demonstration system.

Fig. 4(c) demonstrates exponential tuning of F_{osc} from $30\,\mathrm{Hz}$ to $40\,\mathrm{kHz}$. F_{osc} depends slightly on the envelope set point (V_{sp}) due to OTA nonlinearity, which contributes harmonics of F_{osc} in V_1 and V_2 as seen in Fig. 4(d). Nevertheless, the fundamental is >36 dBVrms above other harmonics.

Fig. 4 also shows the output amplitude fluctuation, THD (computed using ten harmonics), and relative phase versus F_{osc} for two V_{sp} values. Output amplitude variation, which is $\leq \pm 8\%$ over the range of $30\,\mathrm{Hz}$ to $40\,\mathrm{kHz}$, is attributed to envelope detector nonlinearity. Amplitude and phase mismatch between V_1 and V_2 are primarily due to startup and damping OTA placement, which causes an asymmetric TACO design.

Our VCO maintains a THD below 2% when $V_{sp} = 1.20\,\mathrm{V}$. Lower output amplitude improves THD, yet envelope detector ripple mandates a peak-peak output amplitude $\geq 125\,\mathrm{mV}$. THD increases when $100\,\mathrm{Hz} \leq F_{osc} \leq 1\,\mathrm{kHz}$ due to slight output amplitude modulation [see the inset of Fig. 4(f)].

The power draw of the subcircuits on the RAMP are $46\,\mu\mathrm{W}$ at $30\,\mathrm{Hz}$ and $50\,\mu\mathrm{W}$ at $40\,\mathrm{kHz}$; a large portion of this power draw results from current offsets (such as $I_{TR,1}$) and resistive dividers, which are used to interface with off-chip components.

Table I shows a comparison to previous work with amplitude-regulated TACOs providing experimental results. Our VCO possesses the widest reported frequency range of any amplitude-regulated TACO, demonstrating the success of our proposed amplitude control approach in a wideband VCO. Our VCO also possesses low THD and low power draw over its operational range. While the flicker noise of the numerous signal-routing T-gates in the RAMP degrades the phase noise [Fig. 4(e)], the experimental results from this proof-of-concept implementation demonstrate the capabilities of the proposed designs in sensitive, audio-frequency applications, and performance would improve in an application-specific IC.

VI. Conclusion

This work presents a low-power sine VCO that produces an amplitude-controlled, quadrature output in the audio range. VCO subcircuits are theoretically motivated and experimentally verified using an in-house FPAA. Overall, the proof-of-concept VCO has low distortion, and low phase error over three frequency decades. A maxima-sampling envelope detector grants this VCO the widest frequency range of an amplitude-controlled TACO thus far (3.1 decade), and performance metrics should improve substantially with a application-specific integrated circuit. Thus, the proposed VCO and its subcircuits can be useful in energy-constrained lock-in amplifiers and other phase-sensitive signal processors.

References

[1] R. Chawla, C. Twigg, and P. Hasler, "An analog modulator/demodulator using a programmable arbitrary waveform generator," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 6106–6109 Vol. 6.

[2] J.-a. Zhang, *High-Speed and High-Performance Direct Digital Frequency Synthesizer Design.* Springer Singapore Pte. Ltd., 2022.

[3] B. Linares-Barranco, A. Rodriguez-Vazquez, E. Sanchez-Sinencio, and J. L. Huertas, "Generation, design and tuning of OTA-C high-frequency sinusoidal oscillators," *IEE Proc. G - Circuits, Devices and Syst.*, vol. 139, no. 5, pp. 557–568, 1992.

[4] B. Linares-Barranco, T. Serrano-Gotarredona, J. Ramos-Martos, J. Ceballos-Caceres, J. M. Mora, and A. Linares-Barranco, "A precise 90° quadrature OTA-C oscillator tunable in the 50-130-MHz range," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 4, p. 649, 2004.

[5] M. Min and T. Parve, "Improvement of lock-in electrical bio-impedance analyzer for implantable medical devices," *IEEE Trans. Instr. Meas.*, vol. 56, no. 3, pp. 968–974, 2007.

[6] M. L. R. Barrios, F. E. H. Montero, J. C. G. Mancilla, and E. P. Marín, "Application of lock-in amplifier on gear diagnosis," *Measurement*, vol. 107, pp. 120–127, 2017.

[7] D. Bhaskar, M. Tripathi, and R. Senani, "Systematic derivation of all possible canonic OTA-C sinusoidal oscillators," *J. Franklin Institute*, vol. 330, no. 5, pp. 885–903, 1993.

[8] T. Serrano-Gotarredona and B. Linares-Barranco, "7-decade tuning range CMOS OTA-C sinusoidal VCO," *Electronics Letters*, vol. 34, no. 17, pp. 1621–1622, 1998.

[9] S.-H. Tu, Y.-S. Hwang, J.-J. Chen, A. M. Soliman, and C.-M. Chang, "OTA-C arbitrary-phase-shift oscillators," *IEEE Trans. Instr. Meas.*, vol. 61, no. 8, pp. 2305–2319, 2012.

[10] K. Odame and P. Hasler, "Theory and design of OTA-C oscillators with native amplitude limiting," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 1, pp. 40–50, 2009.

[11] J. Galan, R. Carvajal, A. Torralba, F. Munoz, and J. Ramirez-Angulo, "A low-power low-voltage OTA-C sinusoidal oscillator with a large tuning range," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 2, pp. 283–291, 2005.

[12] B. Rumberg and D. W. Graham, "A low-power magnitude detector for analysis of transient-rich signals," *IEEE J. Solid-State Circuits*, vol. 47, pp. 676–685, 2012.

[13] B. Rumberg, D. Graham, S. Clites, B. Kelly, M. Navidi, A. Dilello, and V. Kulathumani, "RAMP: Accelerating wireless sensor hardware design with a reconfigurable analog/mixed-signal platform," in *Proc. ACM/IEEE Conf. Inf. Proc. Sensor Net.*. ACM, Apr. 2015, pp. 47–58.

[14] S. Bhattacharyya, S. Andryzcik, and D. W. Graham, "An acoustic vehicle detector and classifier using a reconfigurable analog/mixed-signal platform," *J. Low Power Elec. Appl.*, vol. 10, no. 1, pp. 6–, 2020.

[15] S. Kim, J. Hasler, and S. George, "Integrated floating-gate programming environment for system-level ICs," *IEEE Trans. VLSI Syst.*, vol. 24, no. 6, pp. 2244–2252, 2016.

[16] B. Rumberg, S. Clites, H. Abulaiha, A. DiLello, and D. Graham, "Continuous-time programming of floating-gate transistors for non-volatile analog memory arrays," *J. Low Power Elec. Appl.*, vol. 11, no. 1, 2021.

[17] J. Hasler, "A programmable on-chip Hopf bifurcation circuit," *IEEE Trans. Circuits Syst. I*, pp. 1–11, 2022.

[18] S. Shah, H. Toreyin, J. Hasler, and A. Natarajan, "Models and techniques for temperature robust systems on a reconfigurable platform," *J. Low Power Elec. Appl.*, vol. 7, no. 3, pp. 21–, 2017.

[19] A. Dilello, S. Andryzcik, B. M. Kelly, B. Rumberg, and D. W. Graham, "Temperature compensation of floating-gate transistors in field-programmable analog arrays," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2017, pp. 1–4.

[20] J. Hasler, S. Kim, and F. Adil, "Scaling floating-gate devices predicting behavior for programmable and configurable circuits and systems," *J. Low Power Elec. Appl.*, vol. 6, no. 3, 2016.

[21] P. Furth and H. Ommani, "Low-voltage highly-linear transconductor design in subthreshold CMOS," in *Proc. IEEE Midwest Symp. Circuits Syst.*, vol. 1, 1997, pp. 156–159 vol.1.

[22] G. Cowan, R. Melville, and Y. Tsividis, "A VLSI analog computer/digital computer accelerator," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 42–53, 2006.

[23] B. M. Kelly, A. T. DiLello, and D. W. Graham, "Reconfigurable analog preprocessing for efficient asynchronous analog-to-digital conversion," *J. Low Power Elec. Appl.*, vol. 9, no. 3, p. 25, 2019.

[24] J. De Lima, "A linearly-tunable OTA-C sinusoidal oscillator for low-voltage applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2. IEEE, 2002, pp. II–II.