Extrema-Triggered Analog-Digital Conversion for Low-Power Wireless Sensor Nodes

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***Abstract*—Analog-digital converters (ADCs) are critical for processing signals in wireless sensor nodes (WSNs). Yet, the large data rate of uniformly-sampled ADCs during the acquisition of non-stationary signals often cuts deeply into the WSN power budget. To address this issue, we propose an "extrema pulse generator" to trigger ADCs at extrema, reducing the number of data points acquired and transmitted. Circuits are constructed and experimentally evaluated on an in-house SoC field-programmable analog array in a 350 nm CMOS process. The extrema pulse generator, which draws 4.3-12.3 µW (depending on the input bandwidth), can efficiently sample both synthetic and natural signals, and the signals can be reconstructed with low error.**

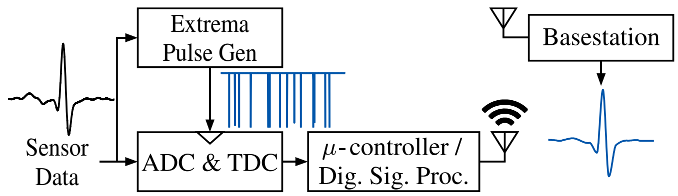

Fig. 1. Signal flow of a potential extrema-triggered WSN. This work proposes the extrema pulse generator (a general-purpose, low-power analog event detector) and demonstrates reconstruction from sampled extrema points.

I. The Need for Intelligent Sampling

Wireless sensor nodes (WSNs) encode physical phenomena into symbols for transmission to a basestation. Designers of WSNs [e.g., Fig. 1] must balance power draw, data quality, and system reconfigurability, which depend on both the input signal and the processing pipeline. Biomedical scenarios, such as implantables and wearables, impose strict resource constraints on WSNs, including power draw and volume [1]–[6]. For example, intracortical neural recorder arrays are limited to $10\,\mathrm{mW}$ to avoid brain tissue damage [7]. In a typical neural recorder power budget, low-noise amplifiers (LNAs) in the analog front end account for 20-30% of the power draw, while analog-digital converters (ADCs) and wireless transmission together account for 40-50% of the power draw [7, 8].

While modern ADCs already perform better than $1\,\mu$W/Mbps [9], simply interfacing with a standard digital output pad with a nominal capacitance of $100\,\mathrm{pF}$ (at VDD=$1\,\mathrm{V}$) necessitates $50\,\mu$W/Mbps. The power draw of ADCs and wireless transmission varies from $100\,\mu$W/Mbps for backscatter communication to $10\,\mathrm{mW}$/Mbps for short-range FSK transmission [7, 8]. Commercial standards like BLE 5 require approximately $50\,\mathrm{mW}$/Mbps at 8 dBm transmission power [10]. Since biological signals, of which electrocardiograms (ECGs) [Fig. 2] are a representative example, are typically nonstationary, nonuniform sampling presents an opportunity to greatly diminish the number transmitted data points at the source. In this way, despite physical constraints on data transmission costs and LNA power draw (limited by gain and noise requirements) [7], nonuniform sampling can mitigate power draw due to nonstationary signal compression and transmission.

This material is based on work partially supported by the National Science Foundation Graduate Research Fellowship under Grant No. DGE-2039655.

This work proposes an "extrema pulse generator," which can trigger a standard ADC (such as an asynchronous successive approximation register) at extrema and a timer to acquire corresponding timestamps [Fig. 1]. Extrema sampling is a widely applicable nonuniform sampling approach, yet it needs the development of more robust hardware and software than are currently available to be used in practice. Compared to previous work [11, 12], which demonstrated low-power extrema detection circuits and reconstruction from extrema points, our work presents several improvements and contributions:

1) Detailed signal-theoretic rationale for extrema sampling.
2) A novel "extrema pulse generator" that can be readily reconfigured for scenarios with different operating frequencies, power budgets, and signal-noise ratios (SNRs).
3) A robust reconstruction algorithm that makes more relaxed assumptions about the interpolation function.
4) *Experimental* demonstration of the Pareto optimality of extrema sampling over uniform sampling.

The extrema pulse generator is constructed and demonstrated using an in-house SoC field-programmable analog array (FPAA) in a $350\,\mathrm{nm}$ CMOS process [13]. This work is organized as follows: Section II enumerates rationales for extrema sampling, Section III describes extrema pulse generator subcircuits, Section IV elucidates reconstruction, Section V demonstrates and compares system performance to other sampling approaches and also provides concluding remarks.

II. The Case for Extrema Sampling

Nonuniform sampling approaches, like the human sensory system, are energy-efficient because they only respond to novel sensory events [17]. These events may include significant changes in input value, as in level-crossing ADCs, or complex

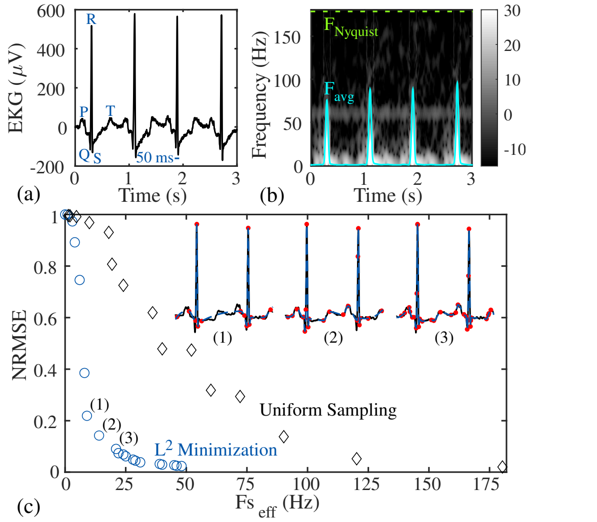

Fig. 2. ECG (a) waveform and (b) wideband spectrogram. Sampling rates $\geq$250 Hz and resolutions $\geq$8 bit are needed to accurately record the sharp features of "QRS complexes" (labeled), which typically last $\leq$20% of the inter-heartbeat period [14, 15]. (c) Pareto fronts [16] for uniform and ideal nonuniform ECG sampling. The nonuniform approach samples time-domain points to minimize polynomial reconstruction error; for PCHIP interpolation, we observe special points, including extrema, enabling the nonuniform approach to reconstruct ECGs more optimally than uniform sampling.

signal features detected through methods like spectral template matching [18], as in application-specific event detectors. The former approach benefits from low component count and high sensitivity (although with low specificity). In contrast, the latter approach achieves higher specificity at the cost of lower sensitivity and a greater number of components. We propose extrema sampling as a general-purpose, middle-ground solution that reduces energy consumption with low component count and low reconstruction error.

Most nonuniform sampling approaches [18]–[24] leverage extra assumptions about signal features (besides the spectral support range) to sample more intelligently. In contrast, extrema sampling relaxes these assumptions, providing a widely-applicable framework that samples at twice the mean frequency of the input signal, which is often much lower than the global Nyquist rate for nonstationary signals, even after paying a two-fold penalty for also acquiring sample timestamps. Extrema sampling also does not require costly signal reconstruction algorithms and is well-justified [19] because:

1) The quantities of interest for a signal often happen to be extrema values and the time between extrema; in such cases, interpolation may not be necessary [25].
2) Extrema, denoting zero crossings of the signal derivative, carry more information than uniformly-sampled points.
3) Extrema occur in excess of half the Nyquist rate for a bandlimited signal. Alongside rationale (2), there is sufficient information to perfectly reconstruct a bandlimited extrema-sampled signal via Lagrange interpolation variants [19].

Additionally, we propose that extrema sampling naturally arises if time-domain points are selected in an unbiased manner to minimize polynomial reconstruction error under a mean sampling rate constraint (Fs_{tar}). We demonstrate this by formulating and solving the following constrained nonlinear integer programming problem with a genetic algorithm:

$$\arg\min_{\mathbf{\Phi}} \ \text{NRMSE} \ \ s.t. \begin{cases} \frac{1}{n}\sum_i \Phi_i \leq Fs_{tar} \\ \forall \Phi_i \in \{0,1\} \end{cases} \tag{1}$$

where NRMSE $:= \|\mathcal{F}(\mathbf{X},\mathbf{\Phi}) - \mathbf{X}\|_2 / \|\mathbf{X} - \langle \mathbf{X} \rangle\|_2$ measures the error between the raw ECG data vector ($\mathbf{X}$) and data reconstructed using a piecewise cubic Hermite interpolating polynomial (PCHIP) function ($\mathcal{F}$) with a binary vector ($\mathbf{\Phi}$) of length n that decides which of the n elements of $\mathbf{X}$ to sample. As shown in Fig. 2(c), idealized nonuniform sampling tends to prioritize significant extrema, achieving a better tradeoff between NRMSE and the effective sampling rate Fs_{eff} compared to uniform sampling, despite the additional overhead required to record timestamps in the nonuniform case.

III. Extrema Pulse Generator

The extrema pulse generator shown in Fig. 3(a) is a low-power circuit comprising two subcircuits: the extrema detector and the edge detector. The extrema detector changes its state at input extrema, and the edge detector produces an active-low pulse when the output of the extrema detector changes state. To understand overall operation, it is important to first understand the behavior of the hysteretic differentiator (HD).

A. *Hysteretic Differentiator*

Differentiation is necessary to detect extrema; however, conventional linear differentiators have poor noise immunity [17]. Differentiators are fundamentally circuits which are insensitive to the true signal value while being sensitive to the local derivative. The HD [Fig. 3(b)] is a nonlinear circuit [17] that fulfills fundamental differentiator functions while still being noise-resistant. Our extrema detector relies on the HD.

The HD is a voltage follower comprising a highly-nonlinear buffer stage and an operational transconductance amplifier (OTA) G_{HD} driving the buffer stage; the output of G_{HD} is the HD output (V_{hd}). For small HD input (V_c) amplitudes, V_{hd} closely follows V_c due to the buffer stage operating in a locally linear region. However, for large V_c, V_{hd} is sensitive to $\text{sgn}(\partial V_c/\partial t)$, changing steeply at extrema due to the corresponding change in the dominant FET; the nFET dominates when V_c increases, and the pFET dominates when V_c decreases. It is worth noting that floating-gate (FG) pFETs are used for implementing all subcircuit bias currents (such as in G_{HD}) and switches for routing nets within the SoC FPAA.

B. *Extrema Detector*

The extrema detector generates a digital output (V_{comp}) that changes state at significant extrema of V_{in}. The primary function of the HD is also to detect extrema, but the output of a single HD is not digital and may be slow if the extrema are not sharp enough. To create a fast, digital-output extrema detector, two HDs (HD1 and HD2) are cascaded, as shown in Fig. 3(a), and the output of HD2 is compared to HD1. HD1 sharpens the extrema of the input V_{in} so that HD2 can respond faster. This approach requires a larger current bias for the OTA

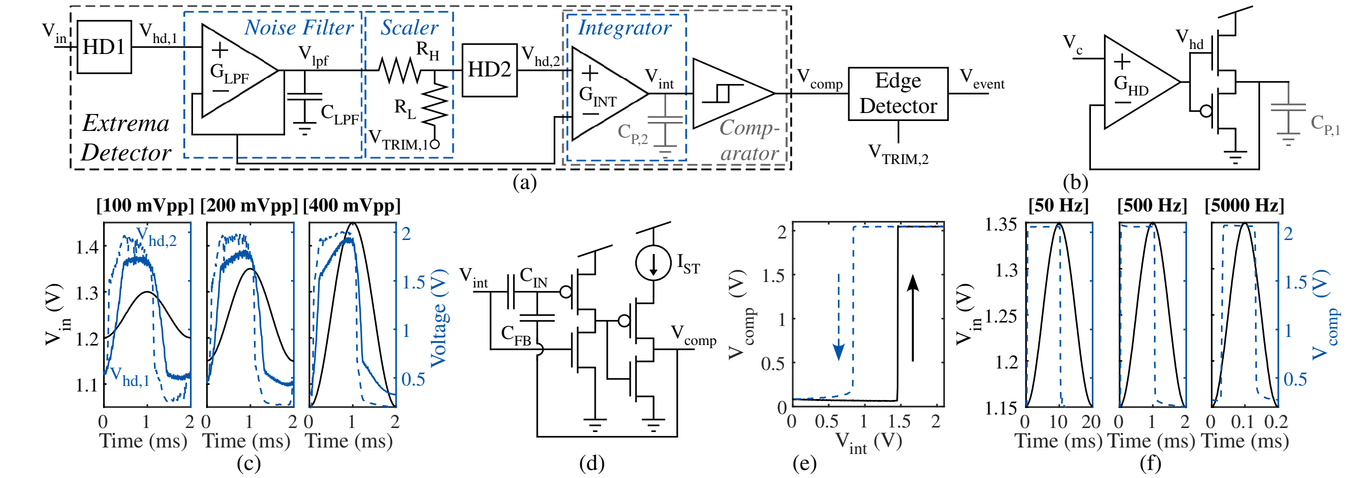

Fig. 3. (a) Extrema pulse generator diagram. (b) HD schematic. (c) Experimental measurements of V_{lpf} and $V_{hd,2}$ responding to 500 Hz sinusoidal inputs of varying amplitudes (increasing left to right). Schmitt trigger (d) schematic and (e) experimentally measured hysteresis curve. (f) Experimentally measured extrema detector response to sinusoids of varying frequencies (increasing left to right). Note that the capacitors in gray are induced through parasitics.

in HD1 to mitigate latency but permits a smaller bias for the OTA in HD2, which incurs a smaller latency penalty.

The other extrema detector subcircuits (the noise filter, scaler, integrator, and Schmitt trigger) compensate for the nonidealities of our approach. The noise filter is a lowpass GmC filter that is adjusted to mitigate HD1 output noise beyond frequencies of interest, which would otherwise be amplified by HD2. The scaler adjusts the input offset (via $V_{TRIM,1}$) and amplitude (via R_H and R_L) of HD2 so that: (1) the output offset of HD1 exceeds the output offset of HD2 by the peak-peak output noise level of HD2, thereby reducing spurious comparisons, and (2) the peak-peak voltage into HD2 does not cause $V_{hd,2}$ to saturate for typical peak-peak values of V_{in}. Figure 3(c) shows V_{lpf} and $V_{hd,2}$ for sinusoids of increasing amplitudes to further elucidate circuit operation.

The integrator and Schmitt trigger compose a noise-immune comparator. The integration rate is tuned such that the comparator state transition time is far less than typical signal periods of V_{in} but greater than undesired noise periods. The Schmitt trigger [Fig. 3(d)] is created by cascading an inverter using an FG pFET with two control gates and a standard current-starved inverter (as suggested in [26]). The Schmitt trigger input (V_{int}) feeds into one control gate (denoted by C_{IN}), and the positive feedback loop of the Schmitt trigger is formed by connecting the output voltage (V_{comp}) to another control gate (denoted by C_{FB}). Since we design complementary FETs to satisfy $\mu_p(W/L)_p \approx \mu_n(W/L)_n$ and with matching threshold voltages, the charge stored in the FG (Q_{FG}) controls the low-high output transition threshold ($V_{T,H}$), while capacitance C_{FB} controls the difference between the high-low ($V_{T,L}$) and low-high ($V_{T,H}$) transition thresholds as shown by the following compact approximations:

$$V_{T,H} \approx \frac{C_T \cdot \mathrm{VDD}}{C_T + C_{IN}} - \frac{Q_{FG}}{C_T + C_{IN}} \tag{2}$$

$$V_{T,H} - V_{T,L} \approx \left(C_{FB} \cdot \mathrm{VDD}\right) / \left(C_T + C_{IN}\right) \tag{3}$$

where $C_T = C_{IN} + C_{FB}$. The Schmitt trigger is tuned so that its hysteresis curve is symmetric about the center of its input range [Fig. 3(e)]. The output of the biased extrema detector, plotted for input sinusoids of different frequencies in Fig. 3(f), has a one latency component that is input-insensitive (from the integrator and Schmitt trigger) and another that increases with increasing input signal period (from the HDs).

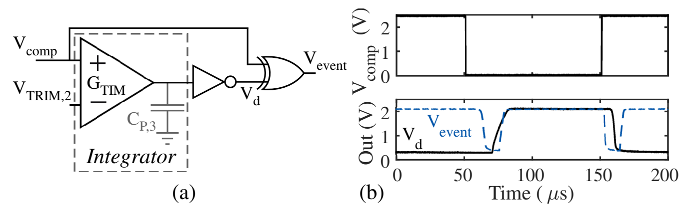

Fig. 4. Edge detector (a) schematic and (b) experimentally measured signals.

C. Edge Detector

The edge detector [Fig. 4(a)] outputs an active-low pulse on each rising or falling edge of its digital input (V_{comp}) [Fig. 4(b)]. The edge detector uses an OTA integrator and a current-starved inverter to generate a delayed and inverted copy of its input. The edge detector then performs an "exclusive OR" of the delayed input (V_d) with V_{comp} to produce output V_{event}.

Integration capacitance ($C_{P,3}$) is produced with interconnect parasitics. The integrator bias (G_{TIM}) is tuned to set a clock pulse width, and the integrator reference, V_{TRIM}, is then adjusted to trim the mismatch between the positive and negative slew rates of the OTA, resulting in matching clock pulse widths for maxima and minima (20 µs in this work).

IV. Reconstruction Algorithm

In this work, extrema (i.e., voltages and corresponding timestamps) are sampled with an 8-bit oscilloscope on the falling edge of V_{event}. Signal reconstruction from these extrema points involves two steps: sample extrapolation and polynomial interpolation. The extrapolation algorithm first uses the neighboring samples to determine if a sampled point is likely to be a local extremum based on non-monotonicity. If the sampled point is likely to be a true local extremum, the extrapolation algorithm corrects the sampled voltage timestamps for the estimated latency of the extrema pulse generator by assuming the input signal is locally sinusoidal. Recall that the

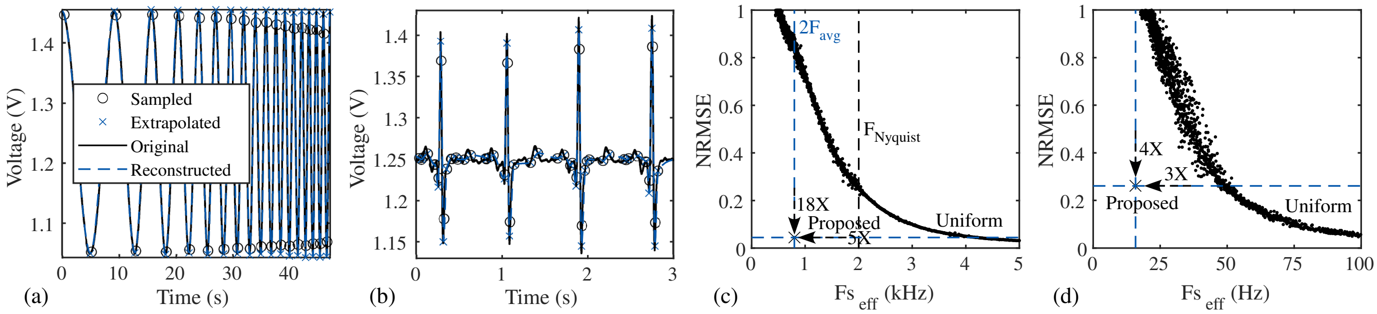

Fig. 5. Experimental results of extrema pulse generator sampling and reconstruction for (a) a quadratic chip and (b) an ECG. The ECG is filtered with a 60 Hz notch before input into the extrema pulse generator. Comparison between uniform sampling and extrema sampling performance for (c) the quadratic chirp and (d) the ECG. Inner points corresponding to the uniform samples form a Pareto front for the uniform approach; extrema sampling is a Pareto improvement.

extrema pulse generator has a latency component that is input-insensitive and a component that increases roughly linearly with the input period; latency for the ambient operating temperature can be characterized using sinusoidal inputs and used to construct a linear model. For each extremum in the sampled data: (1) the timestamps of the previous and next sampled points are used to estimate the local sinusoid period, (2) the delay between the true extrema and the generated clock pulse is estimated from the linear model and subtracted from the measured timestamp, and (3) the true voltage at the extrema is estimated from a parabolic approximation derived from the series expansion of the local sinusoid.

Extrapolated sample points are reconstructed using a polynomial interpolation algorithm to recover the original signal. Lagrange interpolation variants are ideal [19, 27], but can be erratic in the presence of nonidealities (e.g., misalignment of extrapolated extrema, occasional false positives/negatives, etc.), making them difficult to use in practice. PCHIPs [28] are used in this work since they are well-behaved in the presence of timing nonidealities and false positives while preserving extrema locations and having minimal overshoot. Bézier curves with concavity restrictions, as used in [11, 12], only reconstruct well for a limited class of signals.

V. Results, Discussion, and Concluding Remarks

The extrema pulse generator circuits are validated on a SoC FPAA [13] fabricated in a $350\,\mathrm{nm}$ CMOS process, with the scaler circuit external to the FPAA [Fig. 3(a)]. Input voltages are supplied from a function generator in this demonstration system, and extrema are sampled with an oscilloscope on the falling edge of V_{event}. The circuit is optimized and demonstrated separately for two test signals: a quadratic chirp and an ECG. Extrema pulse generator components internal to the FPAA draw $4.3\,\mu\mathrm{W}$ for the ECG and $12.3\,\mu\mathrm{W}$ for the quadratic chirp. Since the power draw of the extrema pulse generator is predominated by the aggregate dissipation of multiple GmC circuits, power draw scales with the input bandwidth requirements, approximately at a rate of $100\,\mathrm{nW/Hz}$.

The quadratic chirp and ECG achieve visually-pleasing reconstructions after sampling [Fig. 5(a-b)], corresponding to NRMSEs of 0.044 and 0.261, respectively. Figures 5(c-d) compare the tradeoff between reconstruction accuracy (NRMSE, which is defined in Section II) and effective sampling rate (Fs_{eff}) between the proposed approach and uniform sampling for the quadratic chirp and ECG. In Fig. 5(c), the proposed approach samples at just twice the average signal frequency (F_{avg}), which is below half the global Nyquist rate of the quadratic chirp, while achieving low reconstruction error. In fact, the uniform approach must sample five times faster to achieve the same reconstruction accuracy, and for the same effective sampling rate (Fs_{eff}), the uniform approach has 18 times higher NRMSE. Similarly, for the ECG [Fig. 5(d)], the uniform approach must sample three times faster to achieve the same NRMSE as extrema sampling, and for the same Fs_{eff}, the uniform approach has four times higher NRMSE. Even if the overhead of acquiring timestamps is considered, and Fs_{eff} is penalized accordingly, extrema sampling remains a Pareto improvement (i.e., improvement in both objectives: NRMSE and Fs_{eff}) over uniform sampling for both the quadratic chirp and the ECG. However, nonidealities like false positives prevent the extrema pulse generator performance from reaching the ideal Pareto front in Fig. 2(c).

TABLE I
Comparison of Nonuniform Sampling Approaches

	Proposed	[11, 12]	[18]	[23]	[29]
Application	Extrema Det.	Extrema Det.	Acoustic Vehicle Det.	Level-Cross. ADC	Async. Δ-Mod.
Platform	FPAA	FPAA	FPAA	ASIC	ASIC
Process (nm)	350	350	350	130	180
Bandwidth (Hz)	60, 1000	60	1000	4000	250
Power (μW)	4.3, 12.3	4.95	43	6.5	109

Table I compares the performance of the extrema pulse generator with other nonuniform sampling approaches in both FPAAs and ASICs that operate in the audio range and utilize a similar technology node. For a given bandwidth, our general-purpose extrema sampling approach draws less power than other FPAA nonuniform sampling approaches [11, 12, 18]. ASICs [23] can usually achieve better performance, and our performance would also improve in a custom implementation.

Although we found PCHIP reconstruction to perform well, our PCHIPs do not explicitly utilize information on whether the sampled point is a maximum or a minimum. In future work, we seek to improve sample information incorporation during interpolation and to redesign the extrema pulse generator for lower power draw and less dependency between noise immunity and clock delay. Overall, the experimental results demonstrate the potential of extrema sampling as a general-purpose data reduction paradigm in ADCs.

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