# A Six-Transistor Integrate-and-Fire Neuron Enabling Chaotic Dynamics

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***Abstract*—Integrate-and-fire (I&F) neurons used in neuromorphic systems are traditionally optimized for low energy-per-spike and high density, often excluding the complex dynamics of biological neurons. Limited dynamics cause missed opportunities in applications such as modeling time-varying physical systems, where using a small number of neurons with rich nonlinearities can enhance network performance, even when rich neurons incur a marginally higher cost. By adding additional coupling into the gate of one transistor within an I&F neuron, we parsimoniously achieve a highly nonlinear system capable of exhibiting rich dynamics and chaos. The dynamics of this novel neuron include regular spiking, fast spiking, and chaotic chattering, and can be tuned via the neuron parameters and input current. We implement and experimentally demonstrate the behavior of our chaotic neuron and its subcircuits on a 350 nm field-programmable analog array. Experimental insights inform a compact simulation model, which validates experimental results and confirms that the additional coupling incites chaos. Results are corroborated with comparisons to traditional I&F neurons. Our chaotic circuit achieves the lowest area (0.0025 mm$^2$), power draw (1.1-2.6 µW), and transistor count (6T) of any nondriven chaotic system in integrated CMOS thus far. We also demonstrate the utility of our neuron for neuroscience exploration and hardware security.**

***Index Terms*—Integrate-and-Fire Neuron, Floating-Gate, Nonlinear Systems, Chaotic Oscillator, Chattering, Synchronization**

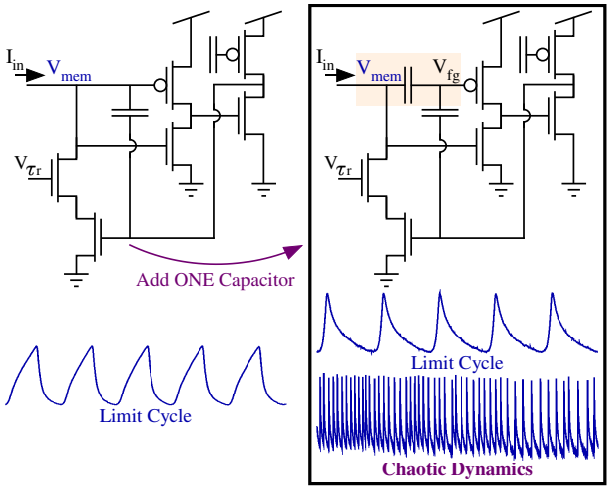


Fig. 1. Integrate-and-fire (I&F) neurons are widely employed in neuromorphic systems but generally lack complex dynamics. This work demonstrates and studies a method to instill rich dynamics, including chaotic chattering, into I&F-style neurons by altering the coupling into the gate of one transistor. This modification facilitates the parsimonious implementation of a highly nonlinear dynamical system, expanding the capabilities of I&F-style neurons.

## I. Introduction of Dynamically-Rich Neurons

THE proliferation of mixed-signal neuromorphic computing systems [1]–[3] underscores a growing interest in leveraging the inherent energy efficiency and real-time output capabilities of analog computation. Contemporary intuition has led to a focus on improving neuron energy-per-spike [4], [5] while maintaining density. Thus, current system designers often opt for integrate-and-fire (I&F) neuron variants as their fundamental compute elements, in effect ignoring important neuron dynamics. Typical I&F neurons lead to missed opportunities in network classification performance due to lacking the complex dynamics observed in their biorealistic counterparts [6]. A properly selected mixture of complex nonlinear neurons can greatly reduce network size while improving modelling of time-varying physical systems [7]. These recent works [6], [7] indicate a shifting paradigm where one can improve both network accuracy and performance-per-Watt by using fewer, yet costlier neurons with biorealistic dynamics.

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The benefits of efficiently modeling biological nonlinearities extends beyond traditional classification tasks and will be crucial for gleaning insight into several neurological diseases, such as Parkinson's disease, Alzheimer's disease, and epilepsy. The complex nonlinear dynamics, including chaotic behaviors [8], exhibited by individual neurons and neural populations are thought to be important for associative memory [9] and population synchronization [10]. From an engineering perspective, chaotic neurons can provide valuable contributions as true random number generators for hardware security [11] and as units in frameworks like reservoir computing [12].

While incorporating dynamical richness into hardware neurons is advantageous, it often results in prohibitively costly implementations that demand large transistor counts or intricate tuning procedures. Moreover, only a few continuous-time chaotic systems have been successfully demonstrated in integrated CMOS, highlighting challenges in the scalable deployment of chaotic neurons. Hence, there is a great need for a hardware neuron model that captures the dynamical richness of biological neurons while addressing practical considerations: ease of tuning, scalability with system size and across technology nodes, back-compatibility with nonchaotic applications, and accessibility to neuromorphic system designers.

In response, this work proposes and experimentally demonstrates a novel six-transistor I&F neuron that enables the

scalable deployment of chaotic neuromorphic systems in integrated CMOS. Our approach involves a seemingly innocuous yet impactful modification to the Mead axon hillock structure [13] widely-adopted by designers; specifically we add a capacitor to alter the gate coupling of one pFET in the architecture (Fig. 1). This modification effectively transforms the pFET into a multi-input translinear element (MITE), a floating-gate (FG) pFET with two control gates, which introduces an additional degree of freedom through a programmable gate charge. Programmability is crucial for the scalability of inherently parameter-sensitive chaotic systems, ensuring robust operation even in the presence of device mismatch. Using a $350\,\mathrm{nm}$ field-programmable analog array (FPAA) developed at Georgia Institute of Technology [14], we experimentally show that our architecture exhibits a diverse range of spiking dynamics, including regular spiking, fast spiking, and chaotic chattering, broadening the scope of I&F neurons. We also provide theoretical analyses to elucidate underlying mechanisms driving chaos. Our contributions are significant and multifaceted:

- *Proposal of a novel neuronal oscillator:* By introducing a single component into the classic I&F neuron, our elegant design achieves the behavioral richness typically associated with far more complex neurons using the fewest transistors, smallest area, and lowest power draw of any non-driven CMOS chaotic circuit to date.
- *Comprehensive experimental characterization in integrated CMOS:* Through more detailed experimental characterization of a FG Schmitt trigger we previously proposed [15] and comparative experimental measurements of traditional and chaotic I&F neurons on the same FPAA substrate, we pinpoint the cause of chaos. The integration of FG technology and use of an FPAA within our design provides the necessary programmability to mitigate mismatch [16], ensuring reliable operation and scaling [17] of inherently parameter-sensitive chaotic systems.
- *Derivation and comparative analysis of a compact neuron simulation model:* We develop and fit parameters to a compact simulation model made publicly available at *github.com/SwagatBhattacharyya/6T_Chaotic_Neuron* to facilitate further research into and adoption of our model.
- *Demonstration of network applications and consideration for ASIC implementations:* We show the integration of our neuron into networks for studying synchronization behaviors inspired by biological systems and for enabling secure hardware communication. We also conceptualize and discuss design considerations for an application-specific integrated circuit (ASIC) implementation.

The rest of this work is organized as follows. Section II examines the current landscape of hardware neurons and implementations of dynamical systems. Section III elucidates circuit architecture and empirically characterizes the chaotic neuron. Section IV presents a compact simulation model and analyzes the factors for chaos. Section V applies our neuron in a network to study synchronization phenomena and demonstrate secure communication. Section VI compares our model to other chaotic systems and discusses further implementation considerations. Section VII offers concluding remarks.

## II. Chaotic Dynamical Systems

While forced chaotic systems need at least two dynamical variables, autonomous chaotic systems require at least three dynamical variables. Chaotic circuit research spans four decades, driven largely by applications in secure communications, where coupled chaotic circuits mask and recover signal spectra, and applications needing random number generation. While a diversity of chaotic systems have been theoretically shown, with attractor shapes including spirals, trumpets, stars, and spikes [18], several challenges have limited the number and types of continuous-time autonomous chaotic systems implemented on CMOS integrated circuits (ICs).

### A. Circuit Implementations of Chaotic Oscillators

While a systematic framework for designing novel chaotic systems is not yet available, chaotic dynamics have been serendipitously observed in several commonplace circuits, including DC-DC converters [19] and Colpitts oscillators [18]. Among contrived chaotic circuits, Chua's circuit is notably prevalent due to its simple state equations, which do not require multiplications. While Chua's circuit is most frequently constructed using discrete components, there have been a few CMOS IC implementations; one adaptation focused on implementing the nonlinear diode [20], while another approach realized the full circuit on an IC by implementing the state equations with integrators, bypassing the need for inductors or gyrators [21]. Unfortunately, circuits with inductive effects are cumbersome to implement on CMOS ICs due to needing a large area for physical inductors or an extensive number of matched transistors for gyrator and state variable emulations.

Other notable implementations of chaotic circuits include third-order jerk circuits employing exponential nonlinearities with diodes [22] and Lorenz systems implemented with a translinear network of MITEs [23]. There has also been recent interest in analog implementations of fractional-order chaotic systems realized using an ample number of filter blocks and multipliers on commercially available FPAAs [24], [25]. When complexity is not a limiting factor, dynamical systems can be embodied using modern general-purpose analog computers, which incorporate integrators, summers, multipliers, and nonlinear elements as demonstrated in [26].

Since the observation of chaos in biological neurons under forced sinusoidal stimuli, there has been considerable interest in developing chaotic neuron models [8]. Most such models are software constructs modified from the classic I&F model. Notably, the quadratic I&F model generalizes the bifurcation properties of conductance-based neuron models near the firing threshold and can be adapted for chaotic dynamics. To this end, [27] introduces an adaptive quadratic I&F neuron exhibiting chaotic behavior. Similarly, [28] introduces a chaotic spiking neuron employing a logistic function, with a model form similar to a modified quadratic I&F neuron.

However, only a few chaotic spiking neuron models have been realized in hardware. Until recently, designs aimed either to approximate [29] or to accurately reproduce [30] Aihara's model [8]. Notably, [30] implemented an asynchronous chaotic spiking neuron in $0.5\,\mu\mathrm{m}$ CMOS, achieving a faithful

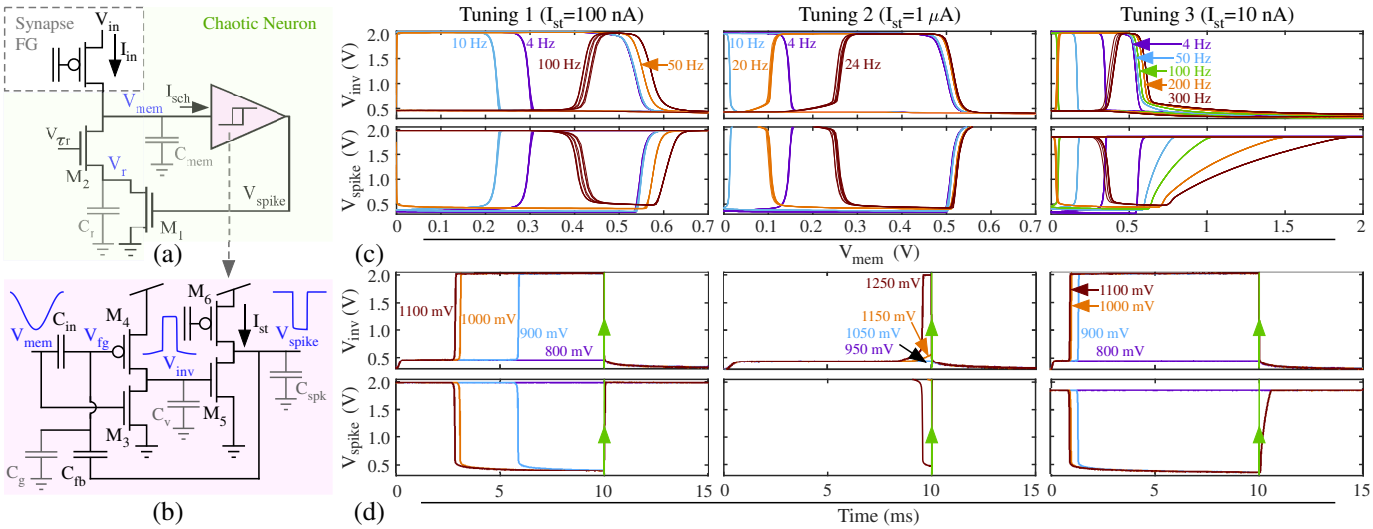


Fig. 2. Schematics of the (a) chaotic neuron driven by an FG synapse and (b) FG Schmitt trigger with parasitic capacitors in gray and nodes in blue. FG Schmitt trigger nodal dynamics elucidated via **experimental** (c) hysteresis curves with $V_{\text{mem}}$ under sinusoidal forcing at varying frequencies and (d) transient responses to 50 Hz $V_{\text{mem}}$ square forcing at varying peak-to-peak amplitudes. In (c-d), we program the MITE so $I_{st}$ =100 nA when control gates are grounded. $I_{st}$ is 100 nA, 1 µA, and 10 nA for Tuning 1, 2, and 3, respectively; we adopt Tuning 1 for the rest of this work. Forced dynamics of the Schmitt trigger, including chaos during high-frequency forcing, are pivotal to neuron behavior, where the interaction of $I_{in}$ and reset mechanism ($M_1$ and $M_2$) regulate $V_{mem}$.

recreation of Aihara's equations in mixed-signal hardware. The design in [30] incorporated smooth nonlinearities, sharp input/output pulses, and time delays, requiring a few hundred transistors and potentially complicating the identification of circuit nonidealities. [29] implemented its model in 2 µm CMOS using a N-shaped piecewise linear approximation for the nonlinearity in Aihara's model. [29] utilized about 70 FETs and a dozen resistors, using half of the available die area. Both [29] and [30] are asynchronous, sampled systems, and can not be definitively classified as non-driven (autonomous). A new type of analog chaotic neuron has been recently proposed [31]. By modifying the two-variable spiking neuron (TSN) in [32], [31] presents a 180 nm CMOS neuron exhibiting a period-doubling route to chaos and behaving like an Izhikevich neuron despite differences in the membrane potential nonlinearity and the coupling between the membrane potential and recovery variable. Nevertheless, [31] uses at least 17 FETs, with several FETs in current mirrors requiring good matching.

### *B. Toward Parsimonious Chaotic Neurons*

Compact mathematical models of neurons rarely translate to compact circuit implementations, and vice versa. We adopt a continuous-time, circuit-driven approach as advocated in [33]. Key insights into parsimonious chaotic neural oscillator design can be gleaned from [34], which utilizes a ring oscillator-like structure with a sgn nonlinearity coupling two adjacent stages. A ring oscillator is similar to a Mead axon hillock that is driven by a constant-current synapse FET, provided there is no feedback capacitor. Another key insight comes from [23], which shows that MITE FG networks can efficiently realize chaotic dynamical systems with nonlinear operations such as division and multiplication. These insights inform the development of our proposed neuron model, which substitutes a MITE FG for a pFET in the first inverter of an axon hillock, reducing feedback capacitance and introducing nonlinear coupling between $V_{mem}$, $V_{inv}$, and $V_{spike}$.

Inclusion of FGs also offers reconfigurability, precision [16], and temperature compensation capabilities [35], which are crucial for robustly implementing inherently parameter-sensitive chaotic systems on modern technology nodes, which have significant process variation and poor control of parasitics. FGs have scaled well to a 40 nm node [17], facilitating the development of cross-technology node standard cell libraries with a high degree of behavioral consistency [36]. By adhering to a few basic design principles, such as employing thick-oxide FETs without gate contacts, FG biases can remain accurate for over 10 years [37]. We deliberately implement our circuits on an FG-enabled, in-house 350 nm SoC FPAA [14] while acknowledging that this may cause minor increases in parasitics compared to an ASIC. In return, the FPAA enables us to use the same FETs for all tests and leverage proven infrastructure to program FGs to 13-bit precision [16] across 98 computational analog blocks (CABs), both of which are necessary for a legitimate comparative analysis of neuron models and biasing conditions.

## III. Experimental Characterization of the Proposed Circuit Architecture

Our neuron is a FG Schmitt trigger circuit with a reset mechanism coupled to its input (Fig. 2(a-b)). The neuron current input $I_{in}$ is generated by applying a voltage $V_{in}$ to the source of an FG synapse FET external to the neuron. The control gates of the input synapse and $M_6$ are connected to a static reference; we do not explicitly depict this extraneous voltage for clarity, as it is taken into account during FG programming to the target runtime drain current. Also note that while the reset mechanism employs a cascode structure, the reset bias in this design $V_{rst}$ is (unconventionally) applied to

the top transistor of the cascode to mitigate the adverse effects of charge injection, which is prominent due to rapid switching induced by the spiking voltage, $V_{spike}$. Since the interaction between $I_{in}$ and the reset mechanism ($M_1$ and $M_2$) forces the voltage on $V_{mem}$, it is imperative to understand the operation and forced dynamics of the Schmitt trigger, since a majority of the behavioral richness of the neuron is encapsulated within.

### A. FG-Enabled Schmitt Trigger

The FG Schmitt trigger (Fig. 2(b)) was initially proposed by [38] and first experimentally shown in [15]. Our version, which is adapted from [15], uses a MITE-based current-starved inverter cascaded with a common-source amplifier. The input of the MITE-based inverter ($V_{mem}$) is tied to nFET $M_3$ and to one control gate of the MITE ($C_{in}$). The other control gate of the MITE ($C_{fb}$) connects to the output of the Schmitt trigger ($V_{spike}$), thereby establishing a positive feedback mechanism. The gate voltage on the MITE pFET ($V_{fg}$), is a weighted sum of the control gate voltages plus a programmable offset. Thus, the integrated positive feedback mechanism makes the switching threshold of the first inverter dependent of the voltage at $V_{spike}$, decreasing the threshold when $V_{spike}$ is high and increasing the threshold when $V_{spike}$ is low.

[15] elucidated two low-frequency properties of the FG Schmitt trigger: the center of the hysteresis window can be adjusted via changing the charge trapped on the FG, and the width of the hysteresis window depends on the capacitive coupling strength from each of the two control gates of the MITE into the channel of $M_4$. However, our approach diverges from previous works in that we: (1) replace the second inverter in the inverter cascade with a common-source amplifier, (2) bias the MITE to operate entirely in subthreshold, and (3) operate the Schmitt trigger far above the frequency where the results from previous works are valid. Thus, we characterize the Schmitt trigger across FG biases and input frequencies to enable a deeper understanding of circuit behavior.

To this end, we first examine the response of the Schmitt trigger dynamical variables to sinusoidal forcing of the input voltage $V_{mem}$ at different frequencies for three tunings (Fig. 2(c)). The settings are as follows: 'Tuning 1': $I_{st}$=100 nA, 'Tuning 2': $I_{st}$=1 µA, and 'Tuning 3': $I_{st}$=10 nA. In all tunings, the MITE is programmed to source ∼100 nA when both of the weakly-coupled control gates are grounded. The net effect of lowering $I_{st}$ is that the operating frequency range of the Schmitt trigger becomes wider; otherwise, the behavior across all tunings is consistent. Compared to the low-frequency hysteresis loops, as the frequency is increased modestly, the lower threshold ($V_{th,L}$) significantly decreases, and the higher threshold ($V_{th,H}$) increases slightly, expanding hysteresis loop width. This expansion is due to the current-starving effect of the MITE, which results in a sluggish low-high transition in $V_{inv}$. At higher frequencies, this sluggish transition can align with the rising input edge, causing an apparent increase in $V_{th,L}$ and an inversion of the slope at the lower edge of the hysteresis loop. At these high input frequencies, we clearly observe forced chaotic behavior. When the input frequency is increased further, all Schmitt trigger nodes saturate.

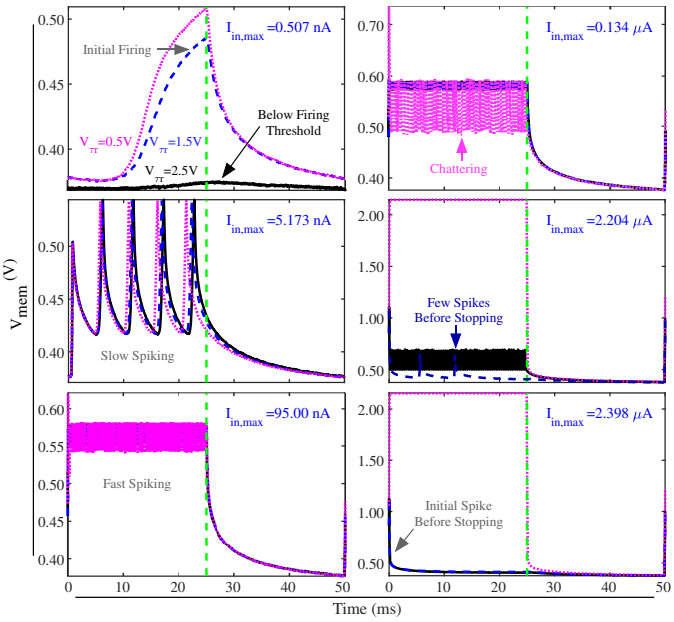


Fig. 3. **Experimental** $V_{mem}$ transient response of the chaotic neuron given 20 Hz input current steps from zero to various $I_{in,max}$ levels. The neuron shows consistent dynamics across $V_{\tau r}$; however, the $I_{in,max}$ for triggering different behaviors, such as initial firing, slow spiking, fast spiking, chattering, and stopping, varies with $V_{\tau r}$. Additionally, under high input currents, $V_{mem}$ latches low at $V_{\tau r} \in \{2.5\,\mathrm{V}, 1.5\,\mathrm{V}\}$ and latches high at $V_{\tau r} = 0.5\,\mathrm{V}$.

Fig. 2(d) shows transient responses of the FG Schmitt trigger voltage nodes to 50 Hz step inputs with varying peak-peak amplitudes, under the same tuning conditions used for the sinusoidal input. At low input amplitudes, the step response of $V_{inv}$ is lowpass, and $V_{spike}$ is saturated. At higher amplitudes, a low-high transition of $V_{inv}$ occurs, and larger amplitudes lead to smaller low-high transition delay. Lowering $I_{st}$ causes the low-high transition of $V_{inv}$ to be faster and of $V_{spike}$ to be slower. We use 'Tuning 1' henceforth due to its wide operating frequency and balance between low- and high-frequency responses, which enables diverse transient behavior.

### B. Dynamics Over Spiking Range

We are now poised to explore the dynamics of the full neuron as a function of the reset bias ($V_{\tau r}$) and input current ($I_{in}$). The initial step involves assessing the transient behavior of the membrane potential $V_{mem}$ when subjected to 20 Hz input steps starting from zero current and stepping to various maximum input current levels ($I_{in,max}$) (Fig. 3). Since the level forced on $V_{spike}$ when $V_{mem}$ is below the Schmitt trigger threshold voltage causes substantial $V_{mem}$-dependent leakage through the reset mechanism, a minimum $I_{in}$ is required to initiate continuous firing. Thus, when $I_{in,max}$ is far below the firing threshold, $V_{mem}$ only modestly increases in response to the input step, albeit with considerable delay, equilibriating when $V_{mem}$ causes leakage to balance $I_{in}$. As $I_{in,max}$ reaches several times the threshold current, the integration rate on $V_{mem}$ increases, sharpening spikes (since rising edges are accelerated) and increasing the spike rate. Increasing spike rates shrink the Schmitt trigger hysteresis window, which diminishes the peak-peak amplitude of $V_{mem}$. As $I_{in,max}$ is

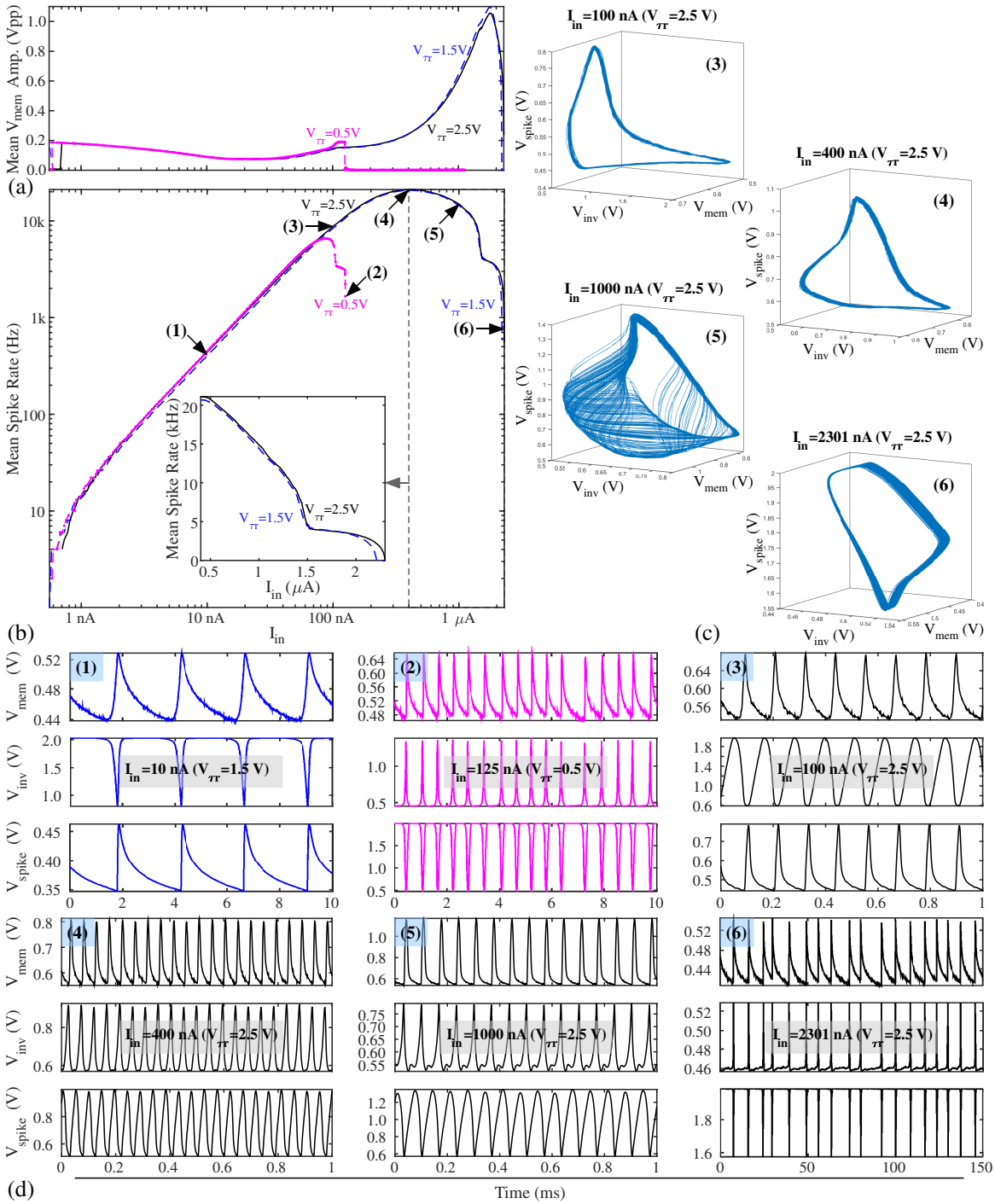


Fig. 4. Chaotic neuron **experimental** measurements. (a) $V_{mem}$ amplitude versus $I_{in}$, (b) annotated IF curve, (c) exemplary attractors in the high input current regime for $V_{\tau r}$ =2.5 V, and (d) nodal voltage waveforms at the exemplary spots annotated on the IF curve. $V_{\tau r}$ alters the threshold current and the point along the IF curve where the response becomes nonlinear, enabling the adjustment of the mean chattering frequency and max frequency through $V_{\tau r}$.

increased further, elevated reset mechanism switching forces the Schmitt trigger into its chaotic regime, where spiking is aperiodic and the spike rate no longer increases consistently with increasing $I_{in}$. When the spike rate drops in the chaotic regime, the spike period percent variation becomes comparatively large, causing chattering.'Chattering' refers to a diversity of rhythmic burst-firing patterns involving brief spike clusters punctuated by short resting periods. Beyond some $I_{in,max}$, continuous firing ceases, with only a few spikes occurring before spiking stops. With further current increases, only an initial spike occurs, as the reset mechanism is unable to sink enough current to initiate a full $V_{mem}$ state transition. After firing ceases, the final value of $V_{mem}$ when the input pulse is applied depends on $V_{\tau r}$; for smaller $V_{\tau r}$, $V_{mem}$ preferentially latches high during the pulse, and for larger $V_{\tau r}$, $V_{mem}$ returns near resting levels after the initial spike.

While Fig. 3 examines the transition from nonspiking states

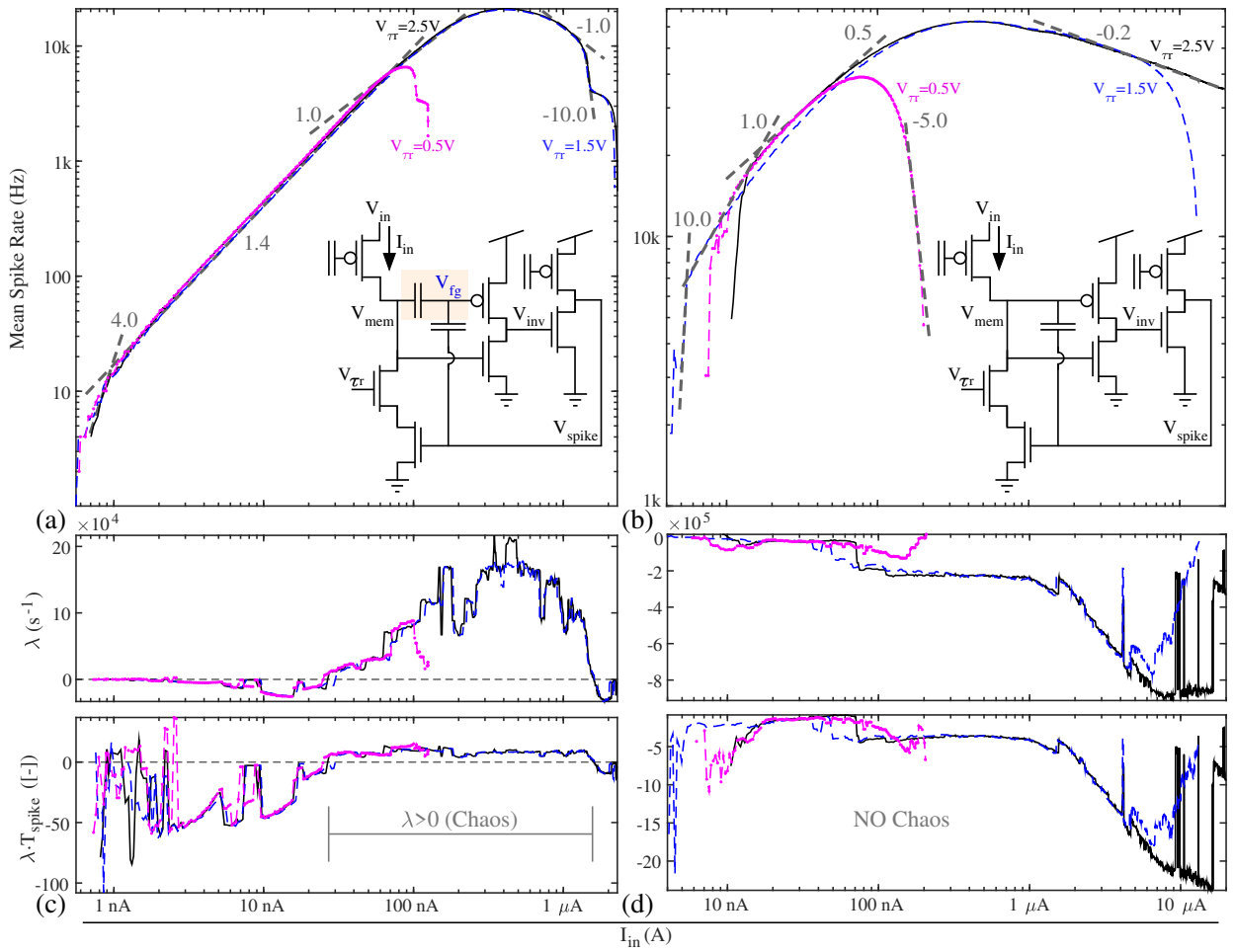


Fig. 5. Comparison of the **experimental** IF curve of (a) the proposed chaotic neuron with (b) a traditional I&F neuron, and **experimental** comparison of the largest Lyapunov exponents of (c) the proposed chaotic neuron and (d) a traditional I&F neuron given constant $I_{in}$. The traditional I&F neuron, which differs from the chaotic neuron in only one capacitor, exhibits strictly negative Lyapunov exponents, whereas the chaotic neuron shows large positive exponents at high $I_{in}$. In (c-d), the bottom row of subplots re-plot the Lyapunov exponents after normalizing by the mean firing rate ($1/T_{spike}$) for visibility.

to spiking states, studying neuron response to static currents better quantifies long-term behaviors after capture by a limit cycle or an attractor. Analyses of responses to transient and static inputs offer complementary insights into how $I_{in}$ and $V_{\tau r}$ shape dynamics. To this end, Fig. 4(a) and Fig. 4(b), depict how $I_{in}$ impacts neuron spike amplitude and frequency, respectively. The curve in Fig. 4(b), which is commonly referred to as an IF curve, shows that the firing rate increases superlinearly until $I_{in}\approx$60 nA for all $V_{\tau r}$ shown. This superlinear increase is caused by a feedback effect – a higher $I_{in}$ increases the $V_{mem}$ integration rate, decreasing the Schmitt trigger hysteresis window, causing the mean spike rate to increase more than proportionately to $I_{in}$. The firing rate peaks at a point (dependent of $V_{\tau r}$) and drops considerably (initially nearly linearly) before the neuron finally stops spiking. $V_{\tau r}$ shifts the point along the IF curve where the curling begins. IF curves mostly overlap before curling begins. As the IF curve curls, we observe several interesting attractors that further corroborate our observation of chaos at high currents (Fig. 4(c)). Fig. 4(d) shows time-domain voltages on these attractors and exemplary waveforms at other points along the IF curve.

Combining complementary insights from Fig. 3 and Fig. 4 provides a more comprehensive understanding of the impact and utility of the degree-of-freedom introduced by $V_{\tau r}$. Reducing $V_{\tau r}$ decreases the $I_{in}$ required to incite spiking and narrows the operating $I_{in}$ range while largely preserving dynamics (except near the threshold currents for initiating and stopping continuous firing). This ability to constrain the $I_{in}$ range, and thereby limit the range of output spike amplitudes and frequencies, adds value during the design of networks of hardware neurons, as it relaxes requirements for presynaptic spike detectors and postsynaptic potential generators [39].

### C. Comparison with Mead-Style Axon Hillock

To elucidate the root cause of chaos in our proposed neuron, we bypass capacitor $C_{in}$, which is equivalent to replacing the MITE with a pFET while retaining the feedback capacitor. The neuron architecture, the CAB components used, and the biasing conditions are otherwise unchanged, thereby transforming our chaotic I&F neuron into a standard I&F neuron (albeit with a common-source output stage instead of the more popular push-pull configuration). We compare the IF curves of both neurons in Fig. 5(a-b). Both curves show a superlinear initial increase in firing rate just past the firing threshold, yet Fig.

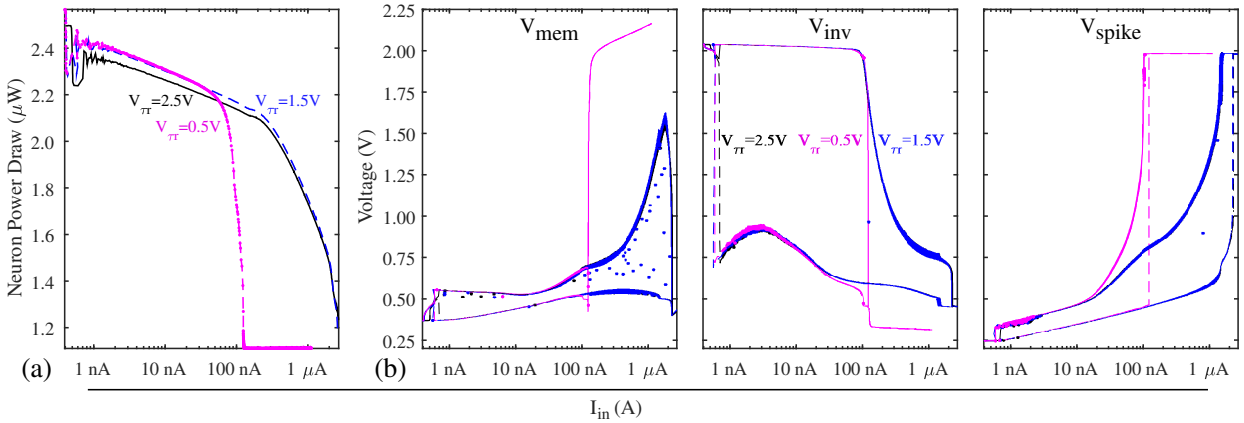


Fig. 6. **Experimental** measurements of chaotic neuron (a) power draw and (b) orbit diagram for the three main dynamical variables as functions of the input current $I_{in}$ and reset bias $V_{\tau r}$. In (b), dashed lines represent minima and solid lines represent maxima. Elevated 'fuzziness' in the orbit diagram indicates cycle-to-cycle amplitude variation, which in turn suggests chaotic behavior, validating results shown in Fig. 5(c-d). In (a), power draw decreases with increasing $I_{in}$ due to the reduced static current contribution from $M_4$ and $M_6$, which drop out of saturation as $V_{mem}$ and $V_{spike}$ increase at high $I_{in}$, as seen in (b).

5(b) shows a linear or sublinear rise across a large range of $I_{in}$ before curling and ceasing to fire. Moreover, the $I_{in}$ at which both IF curves peak for a given $V_{\tau r}$ value is consistent. However, the traditional I&F neuron exhibits a higher firing threshold and higher initial firing rate with a greater sensitivity to $V_{\tau r}$; additionally, the decrease in firing rate prior to stoppage is smoother and spans a broader current range.

We also compare the largest Lyapunov exponents, denoted by $\lambda$, of both neurons (Fig. 5(c-d)). $\lambda$ quantifies the divergence rate of nearby trajectories, distinguishing between chaotic and nonchaotic dynamics. Nonchaotic systems exhibit $\lambda \leq 0$, indicating convergence to limit cycles or quasiperiodicity. In contrast, chaotic systems exhibit $\lambda > 0$ by definition, reflecting sensitivity to initial conditions and unpredictable (yet deterministic) behavior. The deterministic nature of chaos differentiates it from noise, which arises from stochastic processes. Chaos is also unlike instability arising from positive system eigenvalues in that chaotic trajectories remain confined to an attractor. The top row of subplots in Fig. 5(c-d) correspond to the maximal Lyapunov exponents ($\lambda$) estimated from constant-current, time-series spiking data using the MATLAB® 'lyapunovExponent' function. We use an expansion range of $T_{spike}/8$ so the estimated $\lambda$ reflects the immediate trajectory divergence rate. $T_{spike}$ denotes the interspike period, which is the inverse of the mean firing rate. The bottom row of subplots shows $\lambda \cdot T_{spike}$, representing a dimensionless Lyapunov exponent normalized by the firing rate. We observe that the largest Lyapunov exponent of the chaotic neuron transitions from negative to positive values as $I_{in}$ is increased, indicating a transition to chaos. In contrast, the maximal Lyapunov exponent of the standard I&F neuron is always negative. Both neurons exhibit a sizable region where $\lambda T_{spike}$ remains roughly constant despite varying $I_{in}$. In the region with flat $\lambda T_{spike}$, $\lambda > 0$ for the chaotic neuron, and $\lambda < 0$ for the traditional I&F neuron. Both neurons show inflections in $\lambda$ before spiking ceases. Our experiments implicate the MITE (i.e., the coupling into $M_4$) as the root cause of chaotic dynamics. We now develop a mathematical model to decisively show the observed behavior is neither an artifact of the experimental procedure nor physical noise processes and to investigate dependencies on MITE parameters.

## IV. Circuit Modeling

This section follows the process of [39], finding differential-algebraic equations (DAEs) for our chaotic neuron by balancing currents on each circuit node: $V_{mem}$, $V_{inv}$, $V_{spike}$, $V_r$, and $V_{fg}$, isolating time-dependencies, and discarding terms that are insignificant near the middle of the spiking range. In this way, our compact modeling approach provides valuable insights into the root cause of chaotic behavior and the impact of key parameters, enabling a clearer understanding of the core dynamics while intentionally abstracting real-world complexities, such as mismatch and higher-order nonlinearities.

### A. Time-Dependencies

Current balance yields the following expressions:

$$\dot{V}_{mem} = \left(I_{in} - I_{m1} + C_z \dot{V}_{spike}\right) / U_T (C_{mem} + C_z), \quad (1)$$

$$\dot{V}_{inv} = \left(I_{m4} - I_{m3}\right) / U_T C_v, \quad (2)$$

$$\dot{V}_{spike} = \left(I_{m6} - I_{m5} + C_z \dot{V}_{mem}\right) / U_T \left(C_{spk} + C_z\right), \quad (3)$$

$$\dot{V}_r = \left(I_{m2} - I_{m1}\right) / U_T C_r, \quad (4)$$

where voltages are in thermal voltage ($U_T$) units, and $C_z = 1/(C_{in}^{-1} + C_{fb}^{-1})$. Defining: $C_\alpha^2 = (C_{mem} + C_z)(C_{spk} + C_z) - C_z^2$, and backsubstituting Eq. 3 into Eq. 1, we find that:

$$U_T C_\alpha^2 \dot{V}_{mem} = (I_{in} - I_{m1})(C_{spk} + C_z) + (I_{m6} - I_{m5}) C_z, \quad (5)$$

$$U_T C_\alpha^2 \dot{V}_{spike} = (I_{m6} - I_{m5})(C_{mem} + C_z) + (I_{in} - I_{m1}) C_z. \quad (6)$$

We neglect the second term in Eq. 5-6 since $C_z \ll C_{in}, C_{fb} \ll C_{spk}, C_{mem}$. The voltage on the MITE FG node is given by:

$$V_{fg} = V_{FG0} + \beta_m V_{mem} + \beta_s V_{spike};\ \beta_m \approx \beta_s \ll 1 \text{ by design.} \quad (7)$$

In Eq. 7, $V_{FG0}$, denoting the $V_{fg}$ with both MITE control gates grounded, is used to adjust the effective MITE threshold

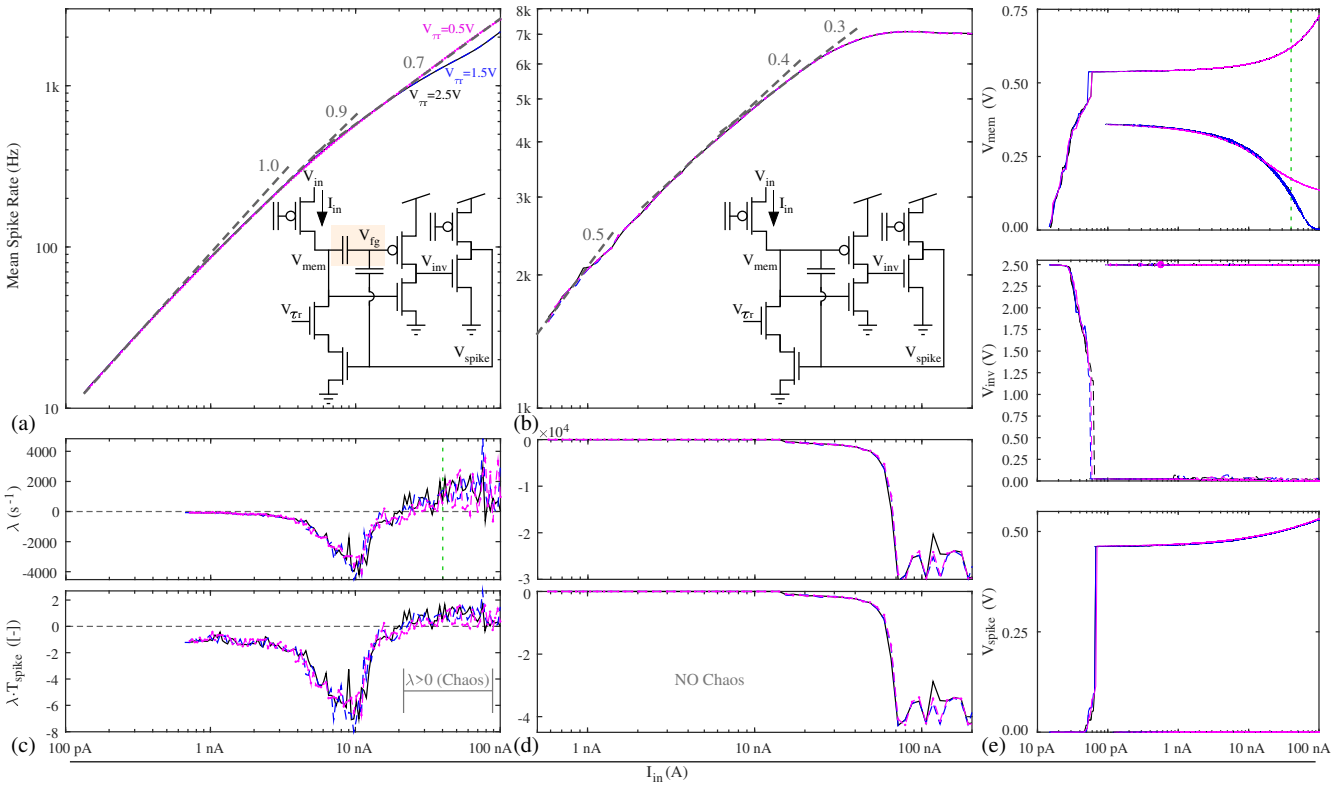


Fig. 7. Comparison of the **simulated** IF curve of (a) the proposed chaotic neuron with (b) a traditional I&F neuron, and numerical comparison of the maximal Lyapunov exponents of (c) the chaotic neuron and (d) a traditional I&F neuron (given constant $I_{in}$). As also observed experimentally, the simulation of the traditional I&F neuron exhibits strictly negative Lyapunov exponents, whereas the chaotic neuron shows positive exponents at sufficiently high $I_{in}$. We evaluate models over the range where assumptions made during development are known to be valid and evaluate Lyapunov exponents only where integration tolerances are met for several oscillation cycles. (d) **Simulated** orbit diagrams for the main dynamical variables in the chaotic neuron.

voltage; in addition, $\beta_m$ and $\beta_s$ denote the capacitive coupling factors looking into $V_{fg}$ from $V_{mem}$ and $V_{spike}$, respectively:

$$\beta_m := C_{in}/(C_{in}+C_{fb}+C_g)\,,\ \beta_s := C_{fb}/(C_{in}+C_{fb}+C_g)\,. \quad (8)$$

### B. Approach for Deriving Transistor Current Expressions

We derive transistor drain currents using the EKV model [13], assuming matched threshold voltage ($V_{t0}$), threshold current ($I_{th}$), and gate-substrate coupling factor ($\kappa$) for all pFETs and nFETs. Note that FETs in our FPAA CABs are designed to approximately match. Our derivations, detailed in Appendix A, leverage experimental insights into the operating regime of each FET during spiking to make valid approximations.

In particular, we first observe that the neuron power draw (Fig. 6(a)) as a function of $V_{\tau r}$ shows a decrease in power draw with increasing $I_{in}$ despite increasing spike rate. This decrease can be attributed to the lower static current through $M_4$ and $M_6$, as the drain-source voltage of $M_4$ and $M_6$ decrease as $I_{in}$ increases. $M_4$ and $M_6$ drain-source voltages can be estimated from the orbit diagrams for $V_{mem}$ and $V_{spike}$, respectively (Fig. 6(b)). In the orbit diagram, dashed lines delineate minima and solid lines delineate maxima. Note that the orbit diagrams appear somewhat fuzzy at high currents, and may have 'detached' minima or maxima (denoted by lone dots), indicating large cycle-to-cycle amplitude variations, in-turn providing another indication of chaos.

### C. Model Summary and IF Curve Fitting Methodology

Compiling findings from Section IV-A and Appendix A:

$$\tau_m \dot{V}_{mem} = I_{in}/\kappa I_{th} - \gamma_1 (V_{mem} - V_r), \quad (9)$$

$$\tau_n \dot{V}_{inv} = \frac{1 - e^{V_{inv}-\mathrm{vdd}}}{e^{\kappa(\beta_m V_{mem}+\beta_s V_{spike})}} - \frac{1 - e^{-V_{inv}}}{\gamma_2 e^{-\kappa V_{mem}}}, \quad (10)$$

$$\tau_s \dot{V}_{spike} = \frac{I_{FGB}}{I_{th}} + \log^2 \frac{1 + E_1 e^{\kappa V_{inv}/2}}{1 + E_1 e^{(\kappa V_{inv} - V_{spike})/2}}, \quad (11)$$

$$\tau_r \dot{V}_r = \left(\kappa\gamma_1/E_1^2\right)(V_{mem} - V_r) - \left(1 - e^{-V_r}\right)/e^{-\kappa V_{spike}}, \quad (12)$$

where $\gamma_2 = \exp(\kappa(\mathrm{vdd} - V_{FG0}))$, $\tau_m = U_T C_\alpha^2/\kappa I_{th}(C_{spk}+C_z)$, $\tau_n = U_T C_v \exp(\kappa(V_{t0}+V_{FG0}-\mathrm{vdd}))/I_{th}$, $\tau_s = U_T C_\alpha^2/I_{th}(C_{mem}+C_z)$, and $\tau_r = U_T C_r \exp(\kappa V_{t0})/I_{th}$. Thus, dynamics are fully determined by a couple key time constants and dimensionless factors, which form a minimal system representation. Certain parameters have little impact on overall behavior if bounded within some range (e.g., $\tau_r$). In the inevitable presence of process variations, such as changes in FET dimensions and nodal capacitances, the degrees-of-freedom provided by the two FGs ($V_{FG0}$ and $I_{FGB}$) as well as $I_{in}$ and $V_{\tau r}$ can be leveraged to make compensatory adjustments to relevant time constants and dimensionless factors to mitigate impact on dynamics.

To fit model parameters, we fix physical constants (vdd and $U_T$) and insensitive parameters ($C_r$, $C_{in}$, and $C_{fb}$), employing a surrogate optimization strategy for the remaining nine pa-

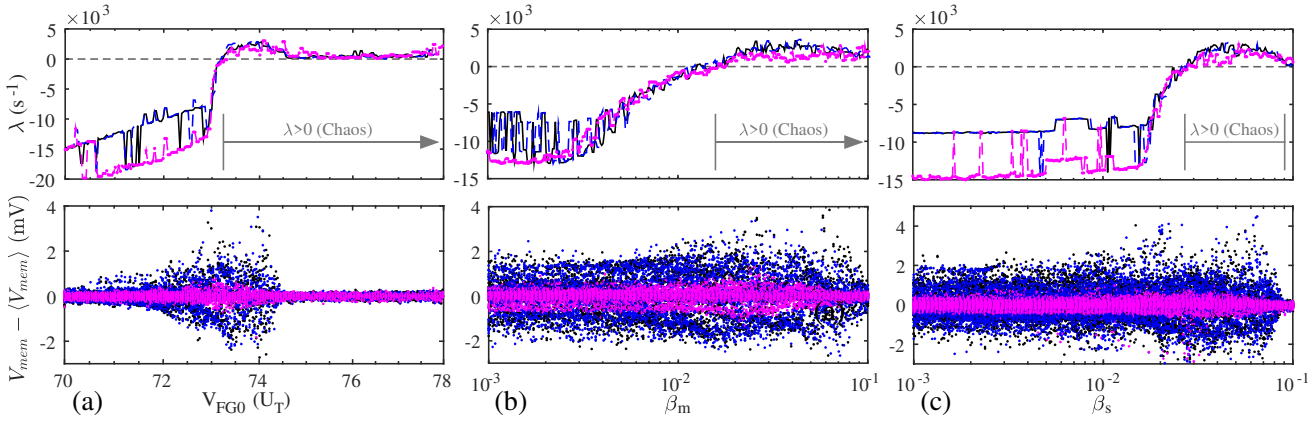


Fig. 8. **Simulated** sensitivity analysis of Lyapunov exponents and deviation of $V_{mem}$ extrema from their mean values as functions of the MITE parameters: (a) $V_{FG0}$, (b) $\beta_m$, and (c) $\beta_s$. Here, $I_{in}$=40 nA (green vertical bars in Fig. 7), and non-swept parameters are fixed to their values in Table I. These plots suggest the Lyapunov exponent is maximized when the MITE is programmed to an optimal bias and if $\beta_m$, $\beta_s$ are above some threshold and close in value.

TABLE I
FITTED NEURON PARAMETERS

| Time Constants | | Dimensionless Factors | | Other Constants | |
|---|---|---|---|---|---|
| $\tau_m$ | 1.326 µs | $\kappa$ | 0.679 | $I_{th}$ | 1.657 µA |
| $\tau_n$ | 0.153 µs | $V_{t0}$ | 18.89 | $I_{FGB}$ | 90.82 nA |
| $\tau_s$ | 0.339 µs | $\beta_m$, $\beta_s$ | 0.065 | $U_T$ | 26.00 mV |
| $\tau_r$ | 5.796 µs | $\gamma_2$ | $3.004\times10^6$ | vdd | 96.00 |

rameters ($\mathbf{X}$). We seek to minimize the mean-squared logarithmic error (MSLE) between the experimental and theoretical IF curves at $n$ query points while maintaining relaxed constraints on parametric range and Lyapunov exponent signage:

$$\arg\min_{\mathbf{X}} \frac{1}{n}\sum_{i=1}^{n} \log^2\left(\left(1+F_t(\mathbf{X},I_{in,i})\right)/\left(1+F_e(I_{in,i})\right)\right) \text{ s.t.}$$
$$\mathbf{X_l}\leq\mathbf{X}\leq\mathbf{X_u},\ \lambda_i<0\,(i\leq i_{z,1}),\ \lambda_i>0\,(i_{z,2}<i<i_{z,3}), \quad (13)$$

where $F_t$ and $F_e$ denote the theoretical and experimental IF curve functions, respectively, and $\mathbf{X_l}$ and $\mathbf{X_u}$ are the parameter bounds. Although its concavity can not be generalized, MSLE is an effective symmetrized percent error-like metric here, since either $F_{t,e}$=0 (e.g., below the spiking threshold), or $F_{t,e} \gg 1$ (in which case, the objective approximates the mean-squared distance between these IF curves on a logarithmic scale). The input current query vector ($\mathbf{I_{in}}$), which spans the spiking range, is a concatenation of two logarithmically spaced halves such that $\lambda$=0 for some $I_{in} \in [I_{in,n/2}, I_{in,n/2+1})$ according to the experimental observations. Therefore, the relaxed Lyapunov exponent constraints must be set up such that: $i_{z,1} < i_{n/2} < i_{z,2}$. The structuring of $\mathbf{I_{in}}$ and the use of a percentage-like objective help balance the fit across both the low-frequency, nonchaotic and high-frequency, chaotic regimes. Optimized parameters are summarized in Table I.

### *D. Model Analysis and Comparison*

We now simulate the IF curve of our chaotic neuron using the optimized parameters over the range where our approximations are valid (Fig. 7(a)). While the concavities of the simulated and experimental IF curve are similar, discrepancies in the firing rate are observed near the edges of the plots. This discrepancy stems from a mismatch between the slopes of the theoretical and experimental IF curves on a log-log scale; near their center, this slope is 1.0 in our simulation, but 1.5 in our experiments. Fig. 7(b) shows the simulated IF curve of a traditional I&F neuron with the same parameters as the chaotic I&F neuron; mathematically, the traditional I&F neuron only differs from the chaotic I&F neuron in that $V_{fg}$=$V_{mem}$, and that the full log-squared form of the EKV models are used for both $M_3$ and $M_4$ as a consequence of larger $V_{mem}$ swings. As in experiment, the initial firing rate of the traditional I&F neuron is higher, and the slope of its IF curve on a log-log scale is roughly half that of the chaotic neuron between its initial and peak rates. We attribute the discrepancy in the IF curve slopes between the models and experimental results to inadequate representation of the following hysteresis effects: frequency-dependent window shrinkage in the chaotic model and feedback capacitance omission in the mathematical model of the traditional I&F neuron (to keep comparisons to the chaotic neuron as close as possible). The hysteresis mechanisms causing these discrepancies are separate from the mechanism inducing chaos as evidenced by the matching shapes and zero-crossings of the Lyapunov exponent curves (Fig. 7(c-d)). Our simulations validate our observations that the Lyapunov exponents of the traditional I&F neuron are always negative, whereas the chaotic I&F neuron exhibits positive Lyapunov exponents at a region of high $I_{in}$. Furthermore, the simulated orbit diagram shapes for the main dynamical variables (Fig. 7(e)) closely match the experimental data.

In our comparative analysis of chaotic and traditional I&F neurons, both experimental and theoretical evaluations pinpoint MITE gate coupling as the cause of chaos. We now investigate the specific nonlinearities responsible for chaos and the optimal parameters to amplify this phenomenon. The chaotic and traditional I&F neurons have distinct feedback mechanisms. In the chaotic neuron, feedback from $V_{spike}$ into the gate of $M_4$ constitutes a voltage-mode weighted sum with $V_{mem}$. In a traditional I&F neuron, this feedback is either an additive, predominantly current-mode feedback when implemented in hardware (and is omitted in our theoretical model without a major change in the dynamics). The expression

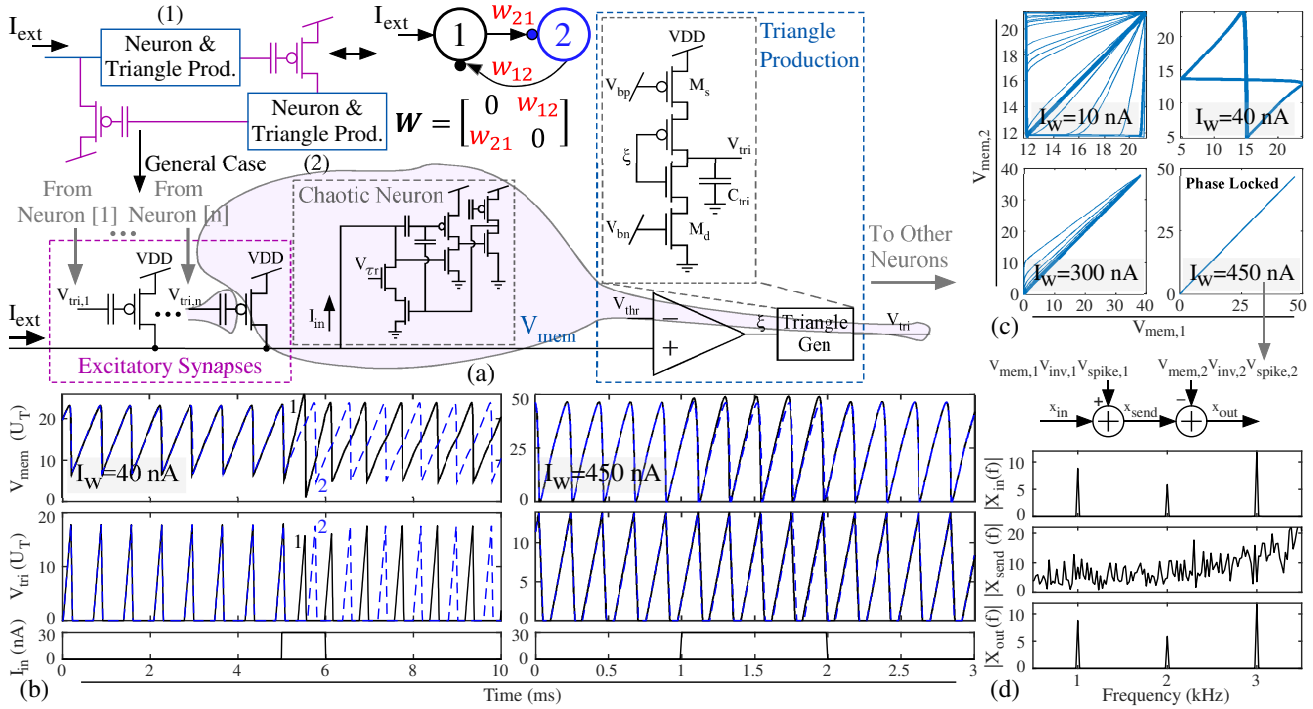


Fig. 9. **Simulations** of a chaotic two-neuron network formed by coupling our neuron model using triangle generators and FG synapses to emulate biorealistic postsynaptic currents. Network (a) signal flow, (b) response to a brief external stimulus under two synaptic weights, and (c) phase portrait after external perturbation, showing phase locking at high synaptic strengths. (d) Use of a phase-locked network ($I_W$=450 nA) to mask and unmask a 'secret message.'

for $\dot{V}_{inv}$ in Eq. 10 is governed by the sum of two terms, where we denote the first term as $T_1$ and the second term as $T_2$. In the chaotic neuron, voltage-mode feedback facilitates interaction between $V_{mem}$ and $V_{spike}$ via the nonlinearity in the denominator of $T_1$, which is a multiplication in small-signal analysis. This nonlinearity is hypothesized as the key to chaos, with expectations of lower Lyapunov exponents if the interaction between $V_{mem}$ and $V_{spike}$ is weaker or if $T_1$ is significantly lower than $T_2$. Given the similar swings of $V_{mem}$ and $V_{spike}$ near the minimum $I_{in}$ needed for chaos, we predict high Lyapunov exponents when $\beta_m \approx \beta_s$ and no chaos when $\beta_m$ and $\beta_s$ are below some threshold. $\gamma_2$, a function of $V_{FG0}$ that grows with increasing MITE bias current, influences the equilibrium of $V_{inv}$, affecting $T_1$ and $T_2$ magnitudes oppositely. Thus, we expect the Lyapunov exponent to peak at some $V_{FG0}$.

We conduct parametric sweeps to validate these hypotheses, performing a sensitivity analysis by varying each of the three MITE parameters: $V_{FG0}$, $\beta_m$, and $\beta_s$ while fixing the input current $I_{in}$ at 40 nA, which is within the chaotic regime and well within the valid range of our model. Our sweeps (Fig. 8) show Lyapunov exponents alongside the distribution of the extrema values of $V_{mem}$ about its min/max levels; while the latter metric can be ambiguous due to persistent integration noise, it serves as a second independent indicator of chaotic behavior. Our findings confirm that chaos is observed if the MITE is programmed to a low current (high $V_{FG0}$), and that the Lyapunov exponent has a distinctive peak. Moreover, we confirm that a minimum $\beta_m$ and $\beta_s$ are necessary to trigger chaos, with the maximal Lyapunov exponents occurring when $\beta_m \approx \beta_s$. These numerical findings give strong support to our hypothesis that the nonlinear denominator of $T_1$ fosters chaos.

## V. Application: Synchronized Chaotic Neurons

We now demonstrate our chaotic neuron in network applications through simulations, showing neural synchronization and secure communication via the circuit-based, two-neuron oscillator design in Fig. 9(a). We prune the framework outlined in [39] to model a two-neuron system using solely excitatory synaptic connections. Interconnection of the neurons involves three steps: (1) detecting presynaptic spikes using a thresholded comparator, (2) generating an asymmetric triangle waveform upon spike detection, and (3) passing the triangle waveform through the FG synapse to produce a biomimetic excitatory postsynaptic current akin to the Rall Alpha function.

While [39] uses switching logic to emulate the functionality of the comparator and triangle generator during derivative computations, our modeling approach adopts a smooth thresholding function using a 'big-$M$' formulation. Our approach enables more efficient simulation of our stiff chaotic systems by addressing the numerical challenges posed by derivative discontinuities. Reformulating Eq. 19 in [39] in terms of the rise rate ($\tau_{tr}$), fall rate ($\tau_{tf}$), and a logistic function ($\sigma(x)=1/[1+\exp(-Mx)]$), triangle evolution is modeled by:

$$\dot{V}_{tri}=\frac{\sigma(V_{mem}-V_{thr})\sigma(\text{vdd}-V_{tri})}{\tau_{tr}}-\frac{\sigma(V_{thr}-V_{mem})\sigma(V_{tri})}{\tau_{tf}}, \quad (14)$$

where $M$ is a large number that abstracts amplifier gains, and $V_{thr}$ denotes the comparator threshold. In this work, $M$=1000,

$\tau_{tr}$=10 µs, and $\tau_{tf}$=2 µs. From [39], the input currents to the neurons given strictly excitatory connectivity are given by:

$$\begin{bmatrix} I_{in,1} \\ I_{in,2} \end{bmatrix} = \boldsymbol{W} \begin{bmatrix} e^{-\kappa_f V_{tri,1}} \\ e^{-\kappa_f V_{tri,2}} \end{bmatrix} + \begin{bmatrix} I_{ext} \\ 0 \end{bmatrix} \text{; Here, } \boldsymbol{W} = \begin{bmatrix} 0 & I_W \\ I_W & 0 \end{bmatrix}. \quad (15)$$

$\kappa_f$, represents the effective control gate-channel coupling of the synapse FG (0.03 here), $I_W$ indicates synapse strength, and $I_{ext}$ denotes an externally supplied perturbation current.

Fig. 9(b) shows the simulated response of the network to a brief external stimulus under two synaptic weights. At $I_W$=40 nA, observe that the stimulus permanently perturbs the relative phases of the neuron, whereas at $I_W$=450 nA, the neurons quickly resynchronize after the disturbance. In the former scenario, the neurons do not truly phase lock, whereas in the latter, they do; Fig. 9(c) shows that the state variables of the two neurons synchronize at a critical synaptic strength. Using such phase-locked chaotic oscillators, one can encode a 'secret' input signal $x_{in}$ by adding the product of the hidden state variables of the first neuron (e.g., $V_{mem,1} \cdot V_{inv,1} \cdot V_{spike,1}$). While it is trivial for the second coupled chaotic neuron to unmask the secret message (since its hidden states closely match those of the first neuron), an outsider lacking knowledge of the neuron internal states (i.e., the ever-evolving 'cipher'), can not unmask the message. This spectral masking method, shown in Fig. 9(d), is a key approach used in chaos-enabled hardware security. Two-neuron oscillators created with nonchaotic neurons, while capable of phase locking [40], lack chaotic dynamics, making them unsuitable for hardware security applications and for enabling simplified analysis of synchronization phenomena in biological networks.

## VI. Discussion

Comparative investigations of our neuron model point to the nonlinear interaction of $V_{mem}$ and $V_{spike}$ in the expression of $\dot{V}_{inv}$, in turn facilitated by the MITE gate coupling, as the root cause for chaotic behavior. This principle can be leveraged to systematically design other chaotic neuron variants tailored to specific application scenarios. Fig. 10(a) shows one such variant, which substitutes the common-source output stage with a current-starved inverter to mitigate static current draw and substitutes the reset mechanism with a T-gate for stronger reset while constraining the design to the components available in a single FPAA CAB. Spike waveforms reveal that this modified circuit retains chaotic behavior and exhibits pronounced bursting dynamics near the stopping current, with longer intervals between spike bursts relative to the short interspike intervals within the bursts. Furthermore, the oscillations and IF curve of this alternative configuration closely resemble those of our originally chaotic neuron, underscoring the robustness and versatility of the FG Schmitt trigger-based design.

To recap, our original six-transistor neuron, which is experimentally demonstrated on a 350 nm FPAA, draws 1.1 µW-2.6 µW (depending on $I_{in}$), achieves spike rates between 2 Hz-20 kHz, and occupies 0.0025 mm$^2$ of the die area, which is estimated by adding the footprints of utilized CAB elements and adding a generous 25% to accommodate interconnect overhead. Comparing our neuron with all previous nondriven

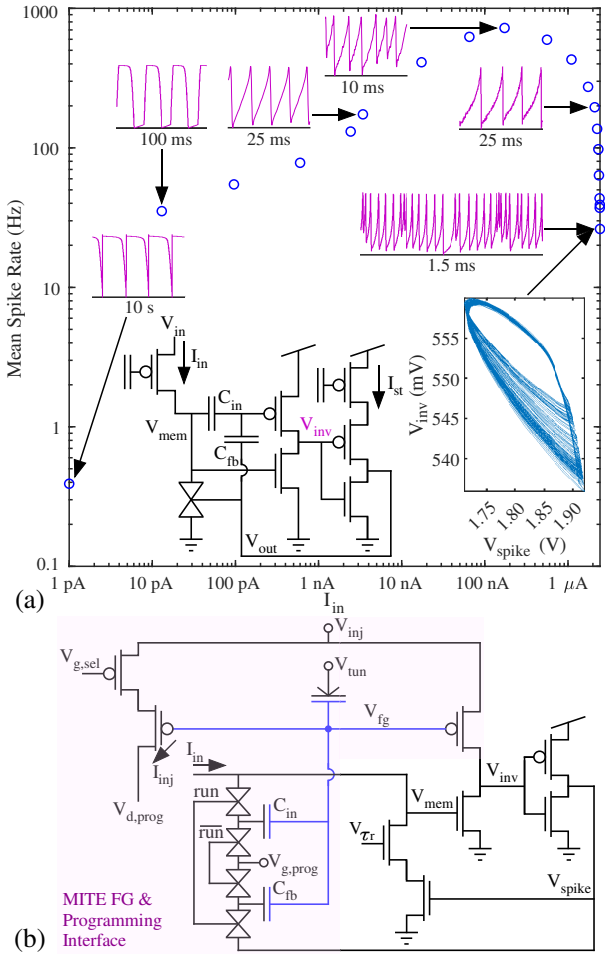


Fig. 10. (a) **Experimental** characterization of an alternative chaotic I&F neuron design using a T-gate reset mechanism and a current-starved inverter in place of a common-source amplifier, mitigating static current. This neuron exhibits an IF curve and oscillations similar to the design shown earlier, but with more pronounced bursting dynamics. (b) Conceptual chaotic neuron design for ASICs, where the $V_{fg}$ net (dark blue) is non-contacted polysilicon.

TABLE II
Comparison of Nondriven Chaotic Systems in Integrated CMOS

| System | Node (nm) | Power (µW) | Frequency | FETs | Area (mm$^2$) |
|---|---|---|---|---|---|
| **Proposed** | 350 | 1.1–2.6 | 2 Hz–20 kHz | 6* | 0.0025 |
| Chua [21] | 2400 | 1600 | 5 MHz | 78 | 0.35 |
| Lorenz [23] | 500 | 2000 | 10 kHz | ∼300 | 0.7 |
| Aihara [29] | 2000 | – | <1 MHz (Est) | 68 | 1.0 (Est) |
| Aihara [30] | 500 | – | <200 kHz | 240 | 0.06 |
| TSN [31] | 180 | – | 0.3-10 kHz (Est) | ≥17 | 0.0075 (Est) |
| Ring Osc [34] | 180** | 29,600† | <150 kHz | ≥16† | – |

*Plus one synapse FET for voltage-mode inputs. **Simulation only with external comparator and capacitors. †Including external comparator.

chaotic systems implemented on CMOS ICs that reported performance (Table II), our proposed chaotic neuron demonstrates the lowest power draw, number of FETs, and area overhead of any such system thus far to the best of our knowledge. The robustness of FGs and EKV models across process nodes ensures consistent scaling of FG-enabled circuits [36]. The reconfigurability, precision, and temperature compensation afforded by FGs are indispensable for modern chaotic neurons.

Transitioning to an ASIC implementation offers significant potential for improving performance metrics, particularly with the development of precise FG programming infrastructure. An ASIC design would reduce routing FETs, mitigating noise effects and parasitics, which in turn decreases extraneous coupling and energy-per-spike. The adoption of an island architecture [41] enables efficient implementation of FG-enabled circuits on ASICs by organizing FG primitives into an abutting crossbar structure with switching and decoding elements at the periphery. The island approach amortizes programming overhead across rows and columns while retaining single-device selectivity, thereby optimizing the density of FG-enabled cells in a 2D grid, reducing place-and-route complexity, and ensuring logical signal flow. Key considerations for FG design include avoiding gate polysilicon contacts, using thick gate oxides to prevent charge leakage and dielectric breakdown, and minimizing tunneling capacitor size.

Fig. 10(b) shows a conceptual chaotic neuron for ASICs using an island architecture. This design adds ten additional FETs to switch the MITE control gates to $V_{g,prog}$ during program mode (when run=0) and to enable indirect hot-electron injection through a program drain [42]. Within an island, program drains ($V_{d,prog}$) are shared among neurons in the same column, gate selection lines ($V_{g,sel}$) are shared across rows, and the tunnel junction ($V_{tun}$) is shared across all neurons. Programming involves switching the island to program mode (run=0), tunneling all FGs in the island, and individually injecting FGs to desired targets. An FG can be selected for injection by asserting $V_{g,sel}$ from a decoder tree and using analog multiplexers to iteratively route the desired drain line to either a pulse voltage source or a logarithmic current-to-digital converter for verification. [16] gives a detailed overview of voltage configurations and timing for tunneling, injection, and intermediate steps, thereby showing the overall approach taken to ensure precise, yet fast programming to a target current.

While our neurons are already resource-efficient, strategically integrating chaotic neurons within heterogeneous networks, where only a portion of neurons show chaotic behavior, can significantly simplify hardware tuning and optimize power and area usage in large-scale systems. Recent research advocates for the use of such heterogeneous networks of complex, nonlinear neurons to drastically reduce network size while enhancing the solution of dynamic modeling problems [7]. Heterogeneous networks require dedicated optimization algorithms for effective weight selection across the network. Our chaotic neuron contributes to a growing body of work promoting the use of fewer, yet more functionally sophisticated neurons with biorealistic dynamics to improve both network accuracy and performance-per-Watt [6], [7].

## VII. Conclusion

This work introduced chaotic dynamics into I&F neurons by changing the coupling into one FET, thereby preserving the core benefits of I&F designs, including ease of tuning and low resource usage, while creating a novel six-FET configuration with complex spiking behaviors, including chaotic chattering. We first characterized and analyzed the behavior of our chaotic neuron and its subcircuits experimentally on an FPAA. We used experimental insights to derive a compact simulation model. Through a comparative analysis of our chaotic neuron with a nonchaotic counterpart through both experiment and simulation, we crossvalidated dynamical observations and analyzed the nonidealities inciting chaotic behavior. Our resource-efficient approach achieves the lowest area, power consumption, and transistor count of any non-driven chaotic system in CMOS, paving the way for scalable solutions in hardware security, reservoir computing, and neuroscience exploration.

## Appendix A
## Derivation of Transistor Current Expressions

Assuming matched pFETs and nFETs, the EKV equation for current out of a pFET drain (well at vdd) is given by:

$$I_p = I_{th}\left[\log^2\left(1+E_p e^{(V_s-\mathrm{vdd})/2}\right)-\log^2\left(1+E_p e^{(V_d-\mathrm{vdd})/2}\right)\right] \text{ where}$$
$$E_p = e^{\kappa(\mathrm{vdd}-V_g-V_{t0})/2} \approx I_{0,p} e^{-\kappa V_g}\left(e^{V_s}-e^{V_d}\right) \text{ [subthreshold]} \quad (16)$$

and into an nFET drain (bulk tied to ground) is given by:

$$I_n = I_{th}\left[\log^2\left(1+E_n e^{-V_s/2}\right)-\log^2\left(1+E_n e^{-V_d/2}\right)\right] \text{ where}$$
$$E_n = e^{\kappa(V_g-V_{t0})/2} \approx I_{0,n} e^{\kappa V_g}\left(e^{-V_s}-e^{-V_d}\right) \text{ [subthreshold]}. \quad (17)$$

In Eq. 16-17, $V_s$, $V_g$, and $V_d$, are $U_T$-normalized source, gate, and drain voltage, respectively. Furthermore:

$$I_{0,p} = I_{th}\exp\left(\kappa\left(\mathrm{vdd}-V_{t0}\right)-\mathrm{vdd}\right),\ I_{0,n} = I_{th}\exp\left(-\kappa V_{t0}\right). \quad (18)$$

We assign currents using information from Fig. 6. To start, $M_6$, which is in subthreshold saturation, supplies its programmed bias $I_{m6}=I_{FGB}$. $M_1$, $M_3$, and $M_4$ are in subthreshold; thus:

$$I_{m1} = I_{0,n}\exp(\kappa V_{spike})(1-\exp(-V_r)), \quad (19)$$
$$I_{m3} = I_{0,n}\exp(\kappa V_{mem})(1-\exp(-V_{inv})), \quad (20)$$
$$I_{m4} = I_{m4,0}\exp(-\kappa V'_{fg})(1-\exp(V_{inv}-\mathrm{vdd})), \text{ where} \quad (21)$$

$I_{m4,0} = I_{th}\exp(\kappa(\mathrm{vdd}-V_{t0}-V_{FG0}))$ and $V'_{fg} = \beta_m V_{mem}+\beta_s V_{spike}$. $M_2$ is typically operated above threshold; thus, defining $E_0 := e^{\kappa(V_{\tau r}-V_{t0})/2} \gg 1$, and factoring the binomial:

$$I_{m2} \approx I_{th}\left[\log^2\left(E_0 e^{-V_r/2}\right)-\log^2\left(E_0 e^{-V_{mem}/2}\right)\right] = I_{th} e^{(V_{mem}-V_r)/2}.$$
$$\log\left(E_0^2 e^{-(V_r+V_{mem})/2}\right) = (I_{th}/4)\left[2\kappa(V_{\tau r}-V_{t0})-V_{mem}-V_r\right]\cdot$$
$$(V_{mem}-V_1) \approx \kappa I_{th}\gamma_1(V_{mem}-V_r);\ \gamma_1 := (V_{\tau r}-V_{t0})/2. \quad (22)$$

Approximations used in Eq. 22 are valid in a subregion of the Ohmic region for which $V_{\tau r}-V_{t0} \gg (V_{mem}+V_r)/2\kappa$, as applicable for biases and frequencies of interest. $M_5$ is also above threshold, but we can not simplify its expression without also affecting model dynamics significantly, thus:

$$I_{m5} = I_{th}\log^2\frac{1+E_1 e^{\kappa V_{inv}/2}}{1+E_1 e^{(\kappa V_{inv}-V_{spike})/2}};\ E_1 = e^{-\kappa V_{t0}/2} \quad (23)$$

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